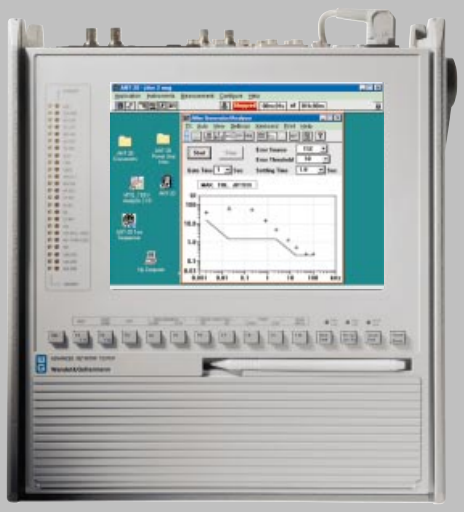
# Leading the Way with Innovative Jitter & Wander Test Solutions


Application Note 71

## Synchronization – Jitter – Wander: Basic principles and test equipment



An ANT-20 application

**Wandel & Goltermann**
Communications Test Solutions

**Abbreviations**

| | |
|---|---|
| ADM | Add Drop Multiplexer |
| ANSI | American National Standards Institute |
| AU | Administrative Unit |
| BITS | Building Integrated Timing Source |
| DS-x | Digital Signal, Level x |
| DWDM | Dense Wavelength Division Multiplex |
| E1 | 2.048 kbit/s link |
| ETSI | European Telecommunication Standardization Institute |
| FAS | Frame Alignment Signal |
| GPS | Global Positioning System |
| GSM | Global System for Mobile Communications |
| ITU | International Telecommunication Union |
| JTF | Jitter Transfer Function |
| LOF | Loss of Frame |
| LOS | Loss of Signal |
| MTIE | Maximum Time Interval Error |
| MTJ | Maximum Tolerable Jitter |
| NDF | New Data Flag |
| NE | Network Element |
| O.171 | ITU-T Recommendation for jitter and wander measurement on electrical interfaces of PDH systems |
| O.172 | ITU-T Recommendation for jitter and wander measurement on electrical & optical interfaces of SDH/SONET systems |
| OC | Optical Carrier |
| PDH | Plesiochronous Digital Hierarchy |
| PLL | Phase Locked Loop |
| POH | Path Overhead |
| ppm | Parts per Million ($10^{-6}$) |
| PRC | Primary Reference Clock |
| PRS | Primary Reference Source |
| RDI | Remote Defect Indication |
| REI | Remote Error Indication |
| RMS | Root Mean Square |
| Rx | Receiver |
| S1 | Synchronization Status Byte (Timing Marker) |
| SDH | Synchronous Digital Hierarchy |
| SEC | SDH Equipment Clock |
| SOH | Section Overhead |
| SONET | Synchronous Optical Network |
| SSU | Synchronization Supply Unit |
| STM | Synchronous Transport Module |
| STS | Synchronous Transport Signal |
| TIE | Time Interval Error |
| TSE | Test Sequence Error |
| TU | Tributary Unit |
| Tx | Transmitter |
| UI | Unit Interval |

**Publishing details**

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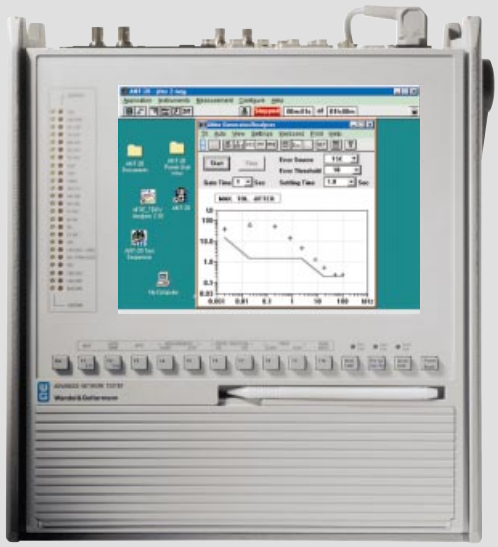
Published by:
Wandel & Goltermann GmbH & Co.
Elektronische Meßtechnik
Mühleweg 5
D-728000 Eningen u. A.
Germany

Subject to change without notice
Order no. TP/EN/A071/0799/AE
Printed in Germany 

**The ANT-20 Advanced Network Tester is the world standard when it comes to transmission test solutions. The ANT-20 is a modular platform offering PDH, SDH, SONET and ATM capabilities, and the instrument can be flexibly configured to handle extremely diverse customer requirements. The jitter test & measurement facilities are one important component:**

- Jitter/wander measurements at all major bit rates (electrical and optical): E1, E3, E4, STM-1/4/16 or DS1, DS2, DS3, STS-1/3/12, OC-1/3/12/48
- Complete compliance with ITU-T Rec. O.172 for comparable, insightful and precise measurement results
- Using the Zoom function, the graphical results presentation format lets you detect errors in the details even with long-term measurements (also useful for acceptance reports)
- Automation with the "CATS Test Sequencer" software increases the efficiency of commonly occurring tests and long-term measurements
- PC-based design, Windows graphical user interface (GUI), touchscreen: Practically any quantity of results and setups can be stored to hard disk. Floppy disk drive for exchanging data. Offline analysis of stored results is possible on any PC. PCMCIA slots simplify installation of modems and/or LAN cards.



## Contents

# 1 Introduction

As we approach the new millennium, the burgeoning demand for information in our modern industrial society keeps the telecommunications industry in constant upheaval. Communications networks must meet ever-growing expectations.

Network operators compete by offering new services (ATM, GSM) with improved performance (low bit error rates, high availability) while delivering more economical solutions based on flexible bandwidth capabilities. These trends have technical consequences, including more expensive transmission techniques, higher data rates and more complex network topologies. Synchronous networks based on SDH/SONET technology are best suited to meeting these requirements, and are now commonplace in transmission applications.

However, these networks make great demands of synchronization and thus the phase stability of clock and data signals.

In real life, various interfering factors prevent perfect synchronization. All systems are subject to “jitter” and/or “wander”, which can cause bit errors, slips, data loss and/or frequency interference, thereby impairing transmission quality. This is why it is so important to verify synchronization during acceptance testing and during regular monitoring of network elements.

# 2 Definition and sources of jitter

## 2.1 What are jitter and wander?

**Jitter**
“Jitter” is the term used to designate periodic or stochastic deviations of the significant instants of a digital signal from the ideal, equidistant values (Fig. 1). Otherwise stated, the transitions of a digital signal invariably occur either too early or too late when compared to a perfect squarewave (reference clock).

**Wander**
Very slow jitter is known as “wander”. ITU-T G.810 puts the limit between jitter and wander at 10 Hz.

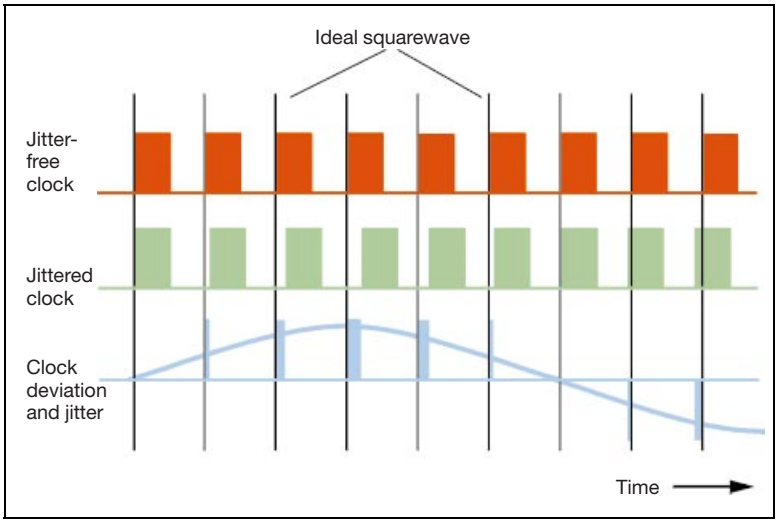



**Fig. 1: Jitter is the deviation of clock transitions from an ideal squarewave**

## 2.2 Sources of jitter and wander

**Interference**
Impulsive noise and crosstalk can produce phase fluctuations composed mainly of higher frequency components, thereby causing non-systematic (stochastic) jitter.

**Pattern jitter**
Digital signal distortion leads to “intersymbol” interference, which is a sort of crosstalk interference between neighboring pulses. Pattern-dependent systematic jitter is the result.

**Phase noise**
Although clock generators are usually synchronized to a reference clock in SDH/ SONET systems, there are still phase fluctuations due to thermal noise or drift in the oscillators, for example. The faster phase variations caused by the noise lead to jitter, whereas the drift caused by temperature variations and aging produces slower phase changes (wander).

**Delay fluctuations**
Changes in the signal delay on a communications path result in corresponding phase fluctuations, which are generally relatively slow. For example, delay variations of this sort occur on an optical fiber due to daily temperature fluctuations. This generally results in wander.

**Stuffing and delay jitter**
During multiplexing, asynchronous digital signals must be adapted to the transmission speed of the higher speed system by inserting stuffing bits. The stuffing bits are removed during the demultiplexing process. The gaps which then occur are evened out by a smoothed clock. This compensation is never perfect, and the result is stuffing and delay jitter.

#### Mapping jitter

Plesiochronous and asynchronous signals are mapped into synchronous containers using stuffing techniques. At the next terminating multiplexer, the plesiochronous tributaries are then unpacked. Due to the stuffing that occurred, there are gaps in the recovered signal, which are compensated using PLL circuitry. There is still some leftover phase modulation, which is known as mapping or stuffing jitter (see section 3.4)

#### Pointer jitter

Clock differences between two networks or between SDH network elements are compensated by pointer movements. These pointer jumps correspond to 8 or 24 bits, depending on the multiplex hierarchy. When the tributary signal is unpacked at the end point, the phase variations are still present but are smoothed out using PLL circuitry. The residual phase modulation is known as pointer jitter. Besides pointer jitter, the unpacked signal also exhibits mapping jitter, so the sum total of both, known as “combined” jitter (see section 3.5), is always measured.

## 2.3 Disruptions caused by jitter

It is the job of clock recovery circuitry used in network elements to correctly sample the digital signal, i.e. as close as possible to the center of the bit, using the recovered bit clock. If the digital signal and the clock both have identical jitter, then the position of the sampling instant does not change despite significant jitter error. Sampling still occurs properly, and no bit errors arise. Strictly speaking, however, this is the case only with low-frequency jitter for which the clock recovery circuitry can keep up with digital signal phase variations with no problems. At higher jitter frequencies, however, the clock recovery circuitry cannot keep up with the fast phase variations of the digital signal. Phase shifts result, and for values $>0.5$ clock periods (UI = Unit Interval), the result is incorrect sampling of the bit element and thus bit errors.

Due to additional digital signal distortion, the decision range is much smaller in real life. At very large jitter amplitudes, bit errors become so common that a loss of frame (LOF) will occur.

## 2.4 Disruptions caused by wander

Unlike jitter, the phase variations due to wander do not lead to bit errors since the recovered clock can easily follow these slow changes in phase. However, wander amplitudes can accumulate to produce very large values over longer time intervals. Digital signals arriving at network and exchange nodes from different directions can have very high wander amplitudes relative to one another. Since digital signals are processed internally with a common clock, buffers are required to compensate for the wander.

At SDH/SONET nodes, these buffers can be relatively small since adaptation is possible using pointer actions. However, pointer actions can lead to a high jitter amplitude in the transported payload signal at the tributary output.

At exchange nodes, however, if the buffer overflows the only way to compensate involves an intentional frame slip. Parts of the transmitted signal are lost, producing error bursts. However, these error bursts do not trigger alarms due to a loss of frame (LOF) or errors in the frame alignment signal (FAS).

## 2.5 How do you measure jitter and wander?

#### Jitter effects

To measure jitter effects, the incoming signal is regenerated to produce a virtually jitter-free signal, which is used for comparison purposes. No external reference clock source is required for jitter measurement. The maximum measurable jitter frequency is a function of the bit rate and ranges at 2.488 Gbit/s (STM-16/OC-48) up to 20 MHz. The unit of jitter amplitude is the unit interval (UI), where 1 UI corresponds to an error of the width of one bit. Test times on the order of minutes are necessary to accurately measure jitter.

#### Wander effects

Wander test equipment requires an external, extremely precise reference clock source. The most practical unit of wander amplitude is the absolute magnitude in ns ($10^{-9}$ seconds), and not the UI unit preferred for jitter measurements. The extremely low frequency components (mHz range) require rather long test times ranging up to $10^{6}$ s.

The differences between jitter and wander are also reflected in the various test applications, even though in both cases we are dealing with phase fluctuations that must be measured and evaluated (Table 1). See section 6 for a basic description of the operation of a jitter/wander test set and a summary of the standards.

| | Jitter | Wander |
|---|---|---|
| Frequency range of phase variations | > 10 Hz | 0–10 Hz |
| Primary disruption | Causes bit errors | Synchronization problems |
| Reference clock source for measurement | Not required | Absolutely necessary |
| Unit for amplitude | UI (Unit Interval) | ns |
| Test times | Minutes | Long-term measurement (hours, days) |

**Table 1: Comparison between jitter and wander, including consequences for test equipment**

# 3 Jitter applications

## 3.1 Measuring output jitter

A certain amount of jitter will appear at the output of a network element even if an entirely jitter-free digital signal or clock is applied to its input. The NE itself produces this “intrinsic” jitter. Reasons are as follows:

- Thermal noise in clock oscillators
- Spurious emissions by crystals in clock oscillators
- Influences from other system modules on the clock supply (crosstalk)
- Pattern-dependent delay in scramblers and encoders
- Insufficient edge steepness in digital signals

Prior to installing network elements, it is important to measure the output jitter to assure that the maximum values are not exceeded (see Appendix, Table 1). This helps avoid interoperability problems with other network elements as well as jitter-related transmission impairments (Fig. 2).

There are separate standards for the output jitter of network interfaces (see Appendix, Table 2), and compliance is important to assure that the jitter tolerance is not violated at any network interfaces. This type of test is particularly important when connecting links/paths between two different network operators. It should therefore be part of any standard acceptance procedure.

The values should be checked within specified jitter bandwidths. There are usually two jitter values: One for high-frequency jitter and one for broadband jitter (see also section 6: “Jitter weighting”)

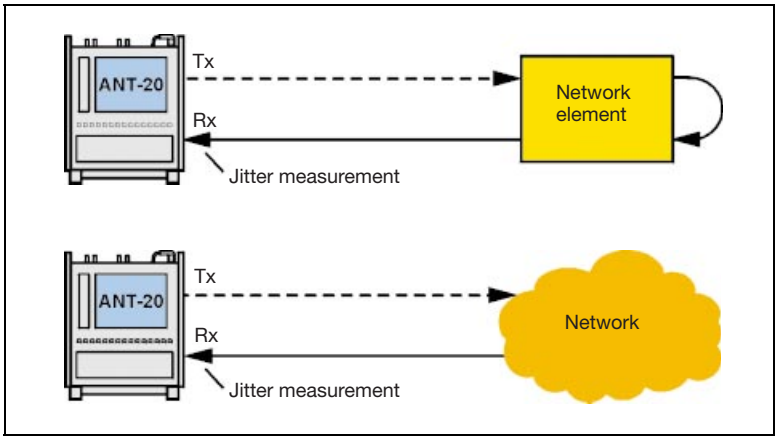



**Fig. 2: Measuring the output jitter of network elements and interfaces**

**Test principle**
The signal under test is connected to the ANT-20’s receiver (Fig. 2). The test set’s transmitter feeds an acceptable signal to the input of the device under test (DUT) in order to prevent an alarm from being triggered. The test duration is variable, i.e. it is not governed by any standards. Experience shows that a duration of 5 minutes works fine. The important parameter here is the maximum peak-to-peak jitter ($UI_{pp}$) during the test interval.

### 3.1.1 Displaying the test results

With its graphical and numerical display facilities, the ANT-20 can show the test results in a table or as a measurement curve, with the following possibilities:

– Current values
– Maximum values within a specific test interval
– Results vs. time

With the many display options, you can systematically analyze and identify reasons for increased jitter and correlate the jitter with transmission errors (Figs. 3 and 4). See the box on p. 7 for an explanation of jitter parameters.

**Displaying instantaneous values**

You can measure the peak-to-peak or root mean square (RMS) value of the jitter. Phase hits can also be counted (see terminology on p. 7). Fig. 3 shows how results are presented for a peak-to-peak jitter measurement. The test set determines the positive and negative values for a phase variation (leading and lagging edges). Phase hits are recorded at the same time. The results are updated continuously ("Current Values"). The "Max. Values" occurring during a specific test interval are also noted and displayed at the end of the measurement.

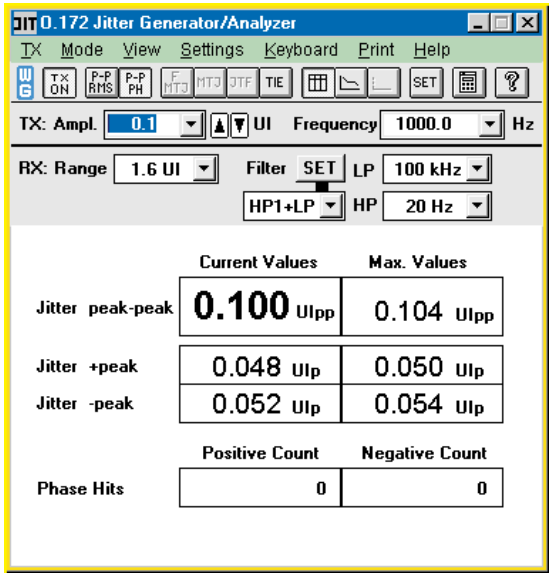



**Fig. 3: Numerical results window showing jitter peak values and phase hits**

**"Jitter vs. time" display mode**

You can record the peak-to-peak or root mean square (RMS) value of the jitter vs. time. This presentation format is particularly useful for long-term in-service monitoring and for troubleshooting. The ANT-20 offers a number of possibilities for in-service analysis. For example, anomalies and defects can be recorded with a time-stamp during a long-term jitter measurement. This helps to correlate increased jitter and transmission errors. The graphics make it easier to identify extreme values. For example, if increased bit errors occur on an operational link, this helps you to systematically identify the problem.

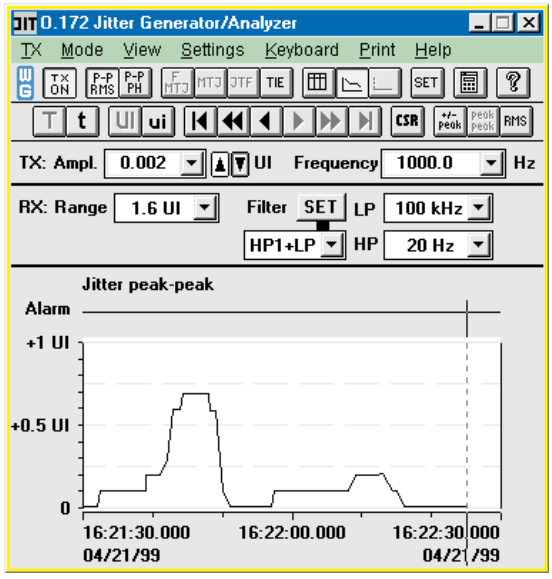



**Fig. 4: The jitter vs. time measurement. Negative and positive peak values can be recorded, or peak-to-peak values.**

## Definition of jitter parameters

**Unit Interval (UI)**
Measure of jitter amplitude. 1 UI corresponds to an amplitude of one bit clock period. The unit interval UI is independent of bit rate and signal coding since it is referred to the length of a clock period.

**Peak-to-peak value**
The distance between the highest and lowest jitter value is known as the jitter amplitude. It is measured as a peak-to-peak value $UI_{pp}$ (Fig. 5).

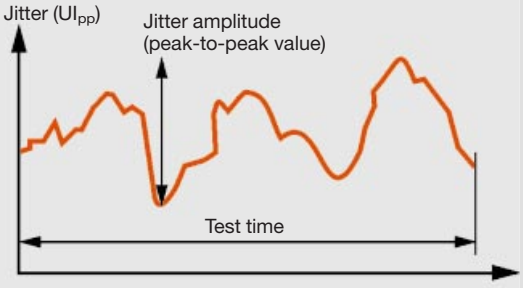



**Fig. 5: Definition of jitter amplitude $UI_{pp}$**

**Phase hits**
A measurement of peak-to-peak jitter says nothing about how often the tolerable jitter amplitudes are exceeded. Phase hits are jitter peaks that exceed an (adjustable) amplitude. Based on a count of phase hits, you can better evaluate jitter behavior. The "Jitter vs. time" presentation also shows how phase hits are distributed over time (see Fig. 4).

**RMS jitter**
The root mean square (RMS) value of the jitter signal provides an indication of the jitter noise power. Peak values that cause bit errors are not recorded by an RMS measurement. Only the quadratic mean is obtained, but the integration time is not standardized. Some standards (e.g. ITU-T G.958, ANSI T1.105.03) use RMS measurement to characterize regenerators (see example below).

## Example: Jitter accumulation in regenerators

Regenerators generally do not use the same precision clock sources as other network elements. Accordingly, jitter is not so highly suppressed. This means that in a chain of generators, jitter can accumulate to yield values which can exceed tolerable limits in some cases.

The RMS value is useful for qualifying the intrinsic jitter of regenerators. Assuming the jitter is non-systematic, the "power law" can be invoked, meaning you can simply add the individual jitter power components for each regenerator in the chain.

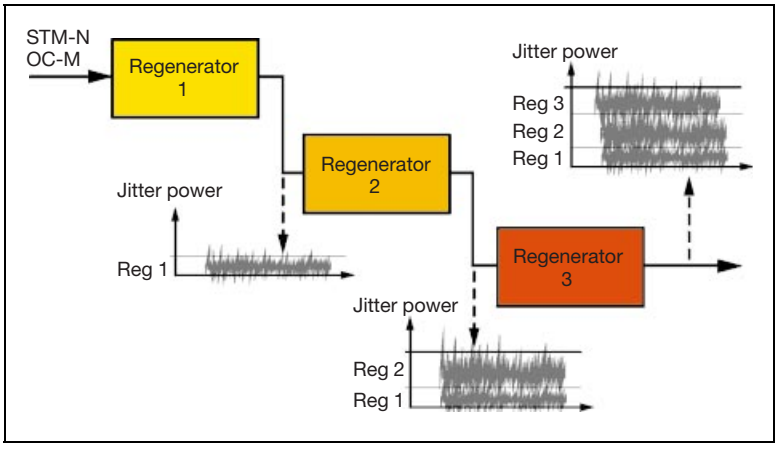



**Fig. 6: The jitter accumulation for a chain of regenerators is computed by adding the RMS values ("power law")**

The RMS value of the jitter at the output of a chain of N regenerators can be computed based on the following formula:

$$J = \sqrt{J_{REG1}^2 + J_{REG2}^2 + \ldots + J_{REGN}^2}$$

For N identical regenerators, the formula can be simplified:

$$J = \sqrt{N} \cdot J_{REG}$$

Now we can compute the maximum tolerable jitter value for a regenerator to avoid exceeding the maximum jitter ($J_{max}$) at the end of a chain of N regenerators:

$$J_{REG} = J_{max} / \sqrt{N}$$ (N = Number of regenerators)

The maximum tolerable output jitter for network elements and networks is given in the Appendix (Tables 1 and 2).

## 3.2 Measuring the maximum tolerable jitter (MTJ)

The optical and electrical inputs of transmission and tributary interfaces must be able to tolerate specific jitter amplitudes (MTJ, maximum tolerable jitter) without loss of signal information. Fulfillment of this requirement needs to be demonstrated during the production and installation of network elements.

### 3.2.1 Test principle

The test set feeds a test signal modulated with sinusoidal jitter into the input of the network element (Fig. 7). Error tests are performed on either the transmission or the tributary interface, depending on the network element configuration. If remote error insertion (REI) is available, you can test the return line of the same interface, without a loop-back at the far end (see section 3.2.5).

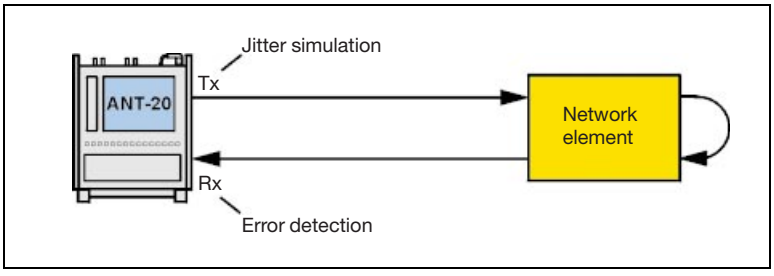



**Fig. 7: Maximum tolerable jitter (MTJ) test on an ADM (transmission interface)**

During the measurement, the jitter amplitude at various jitter frequencies is increased steadily until bit errors exceeding a specific value occur at the output of the network element. The MTJ of the input under test is the maximum jitter amplitude for which the output remains error-free.

The ANT-20 can measure maximum tolerable jitter (MTJ) using an automated algorithm so you can quickly and reliably record the entire measurement curve (involving many single tests). Successive approximation assures that the measurement results are reproducible and that the actual tolerance reserve compared with the limit curve is clearly determined. The instrument begins the test with jitter amplitudes of 50% of the tolerance value. Depending on the result, it then increases or decreases the amplitude by half of the set value until reaching the finest resolution, while allowing the network element a programmable recovery time between measurements.

### 3.2.2 Displaying the test results

The ANT-20 can display the results as a graph or output them as a table of numerical values. The table of values also includes a clear indication of any violations of the limit curve that occur. The existing standard output masks can be altered as required for special applications.

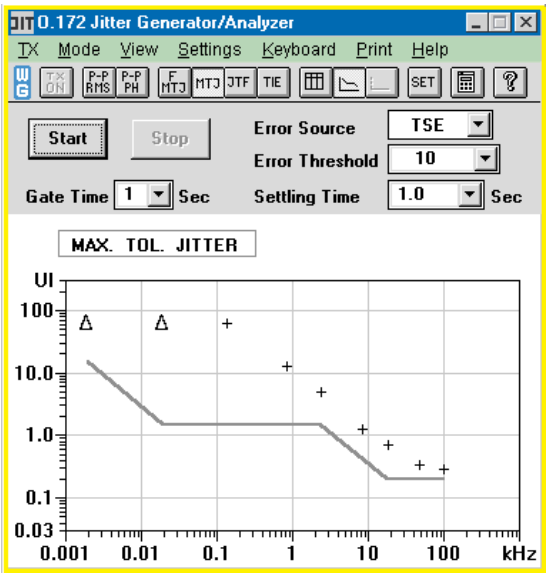



**Fig. 8: Graphical display of results for the MTJ test**

**Note: The test points for MTJ are supposed to lie above the tolerance mask.**

To adapt the MTJ algorithm to the device under test (DUT), you can set the following parameters in the window:

- **Gate Time:** Test interval during which a certain amplitude/frequency combination is present according to the algorithm.
- **Error Source:** Type of error event to be counted during the gate time (usually TSE: Test Sequence Error).
- **Error Threshold:** Adjustable error threshold used as a decision-making criterion by the algorithm.
- **Settling Time:** Recovery time during which a jitter-free signal is provided in order to give the device under test some time to settle after each amplitude/frequency combination.

**Decision-making process of the algorithm:**

If a number of error events (e. g. TSE) exceeding the set threshold occur during the gate time, then the applied amplitude is assumed to be intolerable, i. e. a smaller amplitude must be set during the next step.

### 3.2.3 Fast MTJ measurement

A more rapid assessment of jitter performance of network elements can be made using a quick mask comparison (fast MTJ measurement). This simply sets just the limit curve amplitudes and checks that the output signal is error-free at these amplitudes. The results of this measurement indicate whether the limit curve has been violated, but give no information about the tolerance reserve of the network element's input. The mask can be edited to obtain some reserve with respect to the norm.

### 3.2.4 MTJ measurement with 1 dB *"optical penalty"*

This measurement technique is described, for example, in ITU-T Recommendation O.171 as follows:

- An adjustable attenuator is inserted between the output of the test set (Tx) and the input of the device under test (Rx).
- The optical level is set such that a limit bit error rate of, say, $4 \times 10^{-10}$ is obtained (for example, at STM-16 this BER corresponds to one bit error per second).
- When the level is increased by 1 dB, no more bit errors should occur.
- The MTJ measurement is performed with an error threshold of 1 (TSE) and a gate time of 1 s.

### 3.2.5 MTJ measurements with no loop

Sometimes it is impossible to use bit errors or test sequence errors (TSE) in a test signal for evaluation purposes. In this case, you can use the internal error signaling of the actual network elements. In the jitter generator/analyzer, set the "Error Source" to "REI" and perform an MTJ test.

In this manner, parity violations are detected by SDH/SONET network elements when bit errors occur and reported back as REI, regardless of the content of the data signal. These REIs can be used for MTJ qualification. A good application of this is with ATM network elements since the physical layer in ATM is usually based on SDH/SONET in long-haul applications.

## Definition of the maximum tolerable jitter (MTJ)

Every digital input interface must tolerate a certain amount of jitter without any bit errors or synchronization errors. Tolerance masks are therefore specified for the permissible jitter amplitudes at various jitter frequencies (Figs. 9 and 10). The measurement is made by feeding a digital signal modulated with sinusoidal jitter from the jitter generator to the input of the device under test. A bit error test set monitors the device under test for bit errors and alarms that occur sooner or later when the jitter amplitude is increased. The first occurrence of errors indicates that the maximum tolerable jitter has been reached. If all of these values lie above the tolerance mask, then the jitter tolerance requirement is fulfilled.

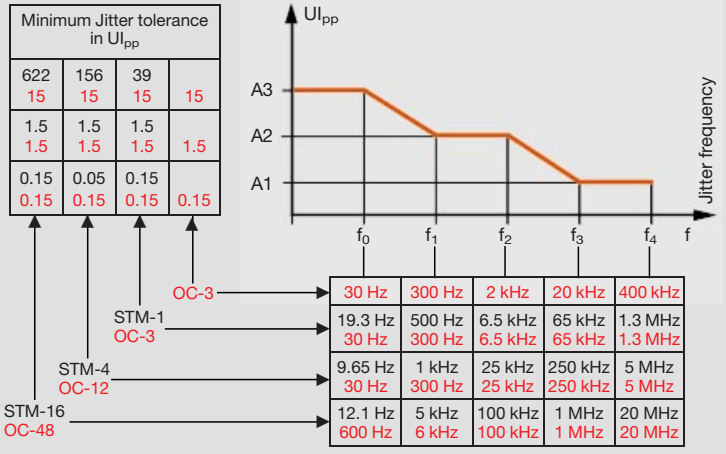



**Fig. 9: Jitter tolerance to G.825, T1.105.03, GR-257, EN302 084**

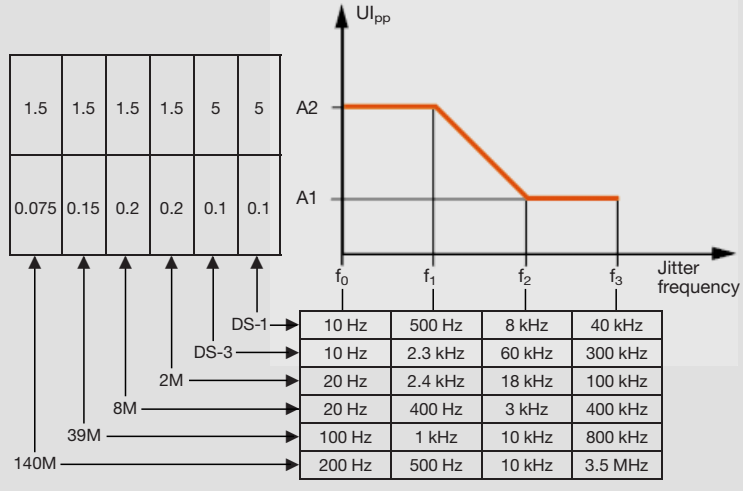



**Fig. 10: Jitter tolerance to G.823, G.824, GR-499**

## 3.3 Measuring the jitter transfer function (JTF)

Intermediate regenerators are required for transmitting signals over long optical paths. These reconstruct the input signal to form a new output signal. Any jitter present at the input will appear at the output as determined by the JTF (jitter transfer function). If the jitter gain is too high, jitter accumulation may occur, leading to violations of the permitted jitter levels. This results in bit errors or signal loss. If JTF is measured early on, this situation can be detected and corrected before it becomes a problem.
A JTF measurement is also necessary when testing DWDM systems.

### 3.3.1 Test principle

The test set feeds a test signal modulated with sinusoidal jitter to the input of the network element under test (in Fig. 11, this is a 2.5 Gbit/s regenerator).

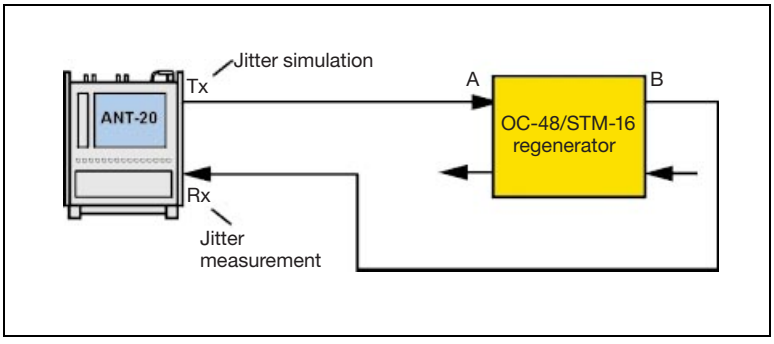



**Fig. 11: Determining the jitter transfer function**

The highest possible jitter amplitude tolerable at the input is selected since a high amplitude results in a better signal-to-noise ratio and thus a more accurate measurement.

The jitter amplitude at the network element output is measured and the JTF calculated from this. The measurement is performed at a number of frequencies in the passband and stopband. The accuracy can be impaired by spurious jitter away from the test frequency, particularly at lower amplitudes. Precise results can be obtained by reducing the spurious influences through narrow-band selection of the test signal.

The ANT-20 has a measurement mode that goes through all the measurement points needed for a fully automatic JTF measurement. This test mode can also include a reference (calibration) measurement.

### 3.3.2 Outputting the measurement results

The results can be output as graphs or tables of numerical values at the press of a key. For special applications, the existing standard output masks can be selected and the output amplitude modified as required (using the “Editor” function).

You can also adjust the settling time, which allows the DUT to settle each time the jitter frequency is changed.

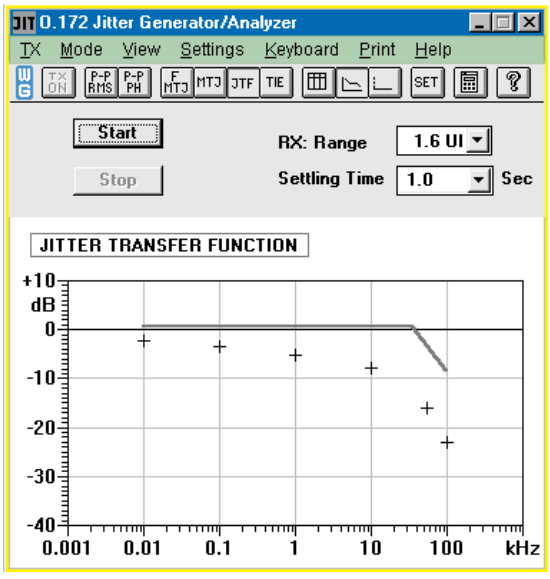



**Fig. 12: Graphical results from an automatic jitter transfer function (JTF) measurement**

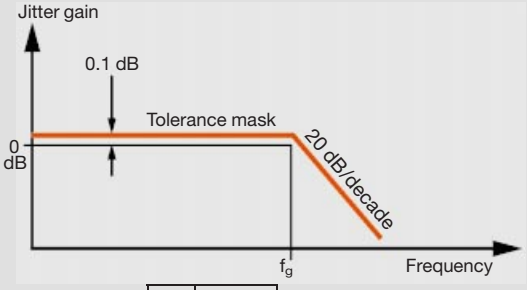
**Note: The test points for JTF are supposed to lie below the tolerance mask.**

### Definition of the jitter transfer function (JTF)

If the input signal to a network element contains jitter, then some component of this jitter can be transferred to the output. The JTF of a network element indicates to what extent the input jitter is transferred to the output, i. e. whether the jitter is amplified or attenuated when passing through the network element. JTF has units of decibels (dB), and is a function of frequency f. It is defined as follows:

$$JTF\,(f) = 20 \cdot \log \left[ \frac{\text{Output jitter (f)}}{\text{Input jitter (f)}} \right]$$

When passing through the network element, the high-frequency components of the jitter are usually suppressed, whilst the low-frequency components are passed unattenuated. In some cases, the input jitter is even slightly amplified. Over a series of regenerators, the jitter can accumulate and exceed the jitter tolerance, thereby producing transmission errors.
To improve the accuracy of the JTF measurement, the intrinsic errors of the test setup should be eliminated using a reference (calibration) measurement prior to connecting the DUT.




| | Type | $f_g$ |
|---|---|---|
| OC-1 | — | 40 kHz |
| STM-1/OC-3 | A | 130 kHz |
| | B | 30 kHz |
| STM-4/OC-12 | A | 500 kHz |
| | B | 30 kHz |
| STM-16/OC-48 | A | 2 MHz |
| | B | 30 kHz |

**Fig. 13: Jitter tolerance for PDH/DSx/SDH/SONET as per ITU-T Rec. G.958 (JTF of STM-N regenerators)**

Typical transfer functions result from the properties of the clock regeneration. Higher jitter tolerance is generally required at low frequencies. In this range, the recovered clock must follow the jitter in order to correctly sample the digital signal at higher jitter amplitudes.
Due to the band limitation of the clock regeneration, higher jitter frequencies are suppressed from the clock signal. The tendency of the clock regenerator to act as a lowpass filter with a cutoff frequency of $f_c$ is reflected in the jitter transfer function.

## 3.4 Measuring the mapping jitter

Plesiochronous and asynchronous signals are mapped into synchronous containers (known as “tributaries” in SONET) using a technique known as stuffing. The plesiochronous tributaries are then unpacked at the next terminating multiplexer. Gaps due to previous bit stuffing occur in the recovered signal. These are compensated for using PLL circuits. Despite this, a certain amount of phase modulation remains. This is known as mapping jitter or stuffing jitter.
The stuffing frequency depends on the system offset of the plesiochronous tributary signal. There are tolerances for the maximum offset at each tributary bit rate (see Table 2, p. 12 for pulling range).

### 3.4.1 Test principle

The ANT-20 transmits a plesiochronous signal to the tributary input of a network element, e. g. an add/drop multiplexer (ADM) in Fig. 14.

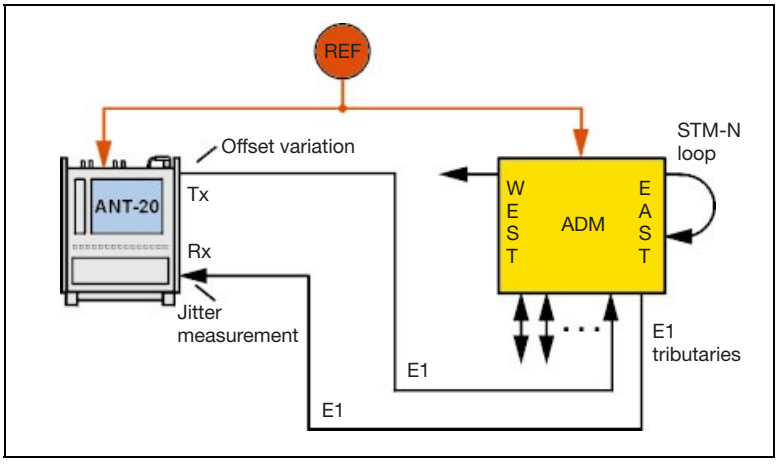



**Fig. 14: Analysis of mapping jitter at tributary outputs**

The tributary is mapped into a synchronous signal in the ADM. At the far end, this synchronous signal is received, the tributary unpacked from it and fed back to the test set. The test set performs jitter analysis on the restored tributary signal using defined filters. The mapping jitter is monitored while the plesiochronous tributary signal is offset in frequency up to the system limits (see Table 2, p. 12). This time-consuming procedure can be automated using a software tool known as the “CATS Test Sequencer”.

To avoid jitter components due to pointer movements, the test set and ADM are synchronized to the same reference clock. This can involve an external reference clock, or you can use the ANT-20’s clock (clock output jack) to synchronize the ADM. With the ANT-20, you can make offsets up to ±500 ppm. The system tolerances are well below this value so you can determine the reserve of the input circuitry (pulling range).

### 3.4.2 Outputting the test results

In this measurement, it is the peak-to-peak jitter results that are relevant. Results are output exactly as they were in section 3.1 “Measuring the output jitter”.

### 3.4.3 Other application

The mapping jitter test is described below as a half-channel measurement (Fig. 15). The ANT-20 transmits a synchronous signal into an aggregate input (here: West), which can be looped back at the other aggregate port (here: East).

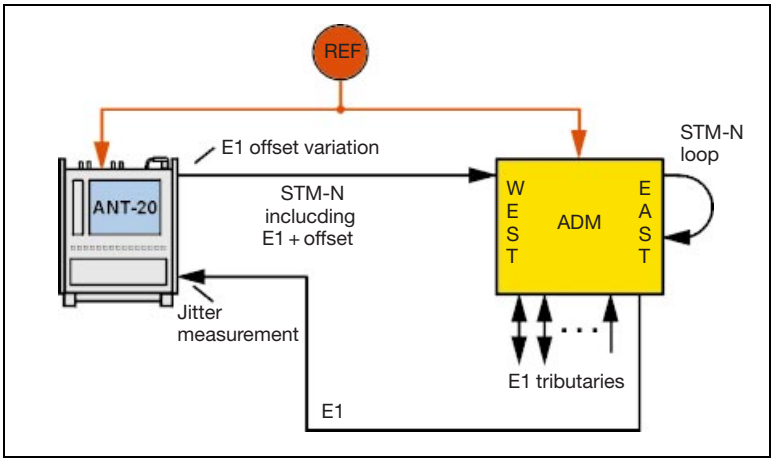



**Fig. 15: Analysis of the mapping jitter on tributaries, performed as a half-channel measurement**

This signal has a plesiochronous tributary test channel mapped into it (e.g. 2 Mbit/s in STM-1), which is unpacked in the network element (ADM) and fed via a tributary output to the test set. On the transmitting end, the test set is now able to offset the transport bit rate of the tributary (±100 ppm). As was the case when analyzing the mapping jitter at the tributary output, the test set and the DUT must be synchronized. ITU-T Rec. G.783 defines the allowable mapping jitter. (Table 2).

| Bit rate | Max. offset | Max. jitter (p-p) | Highpass | Lowpass |
|---|---|---|---|---|
| 1.544 Mbit/s (DS1) | ±50 ppm | 0.1 UI | 8 kHz | 40 kHz |
| 2.048 Mbit/s (E1) | ±50 ppm | 0.075 UI | 18 kHz | 100 kHz |
| 34.368 Mbit/s (E3) | ±30 ppm | 0.075 UI | 10 kHz | 800 kHz |
| 44.736 Mbit/s (DS3) | ±20 ppm | 0.1 UI | 30 kHz | 400 kHz |
| 139.264 Mbit/s (E4) | ±15 ppm | 0.075 UI | 10 kHz | 3500 kHz |

**Table 2: Maximum mapping jitter as per ITU-T G.783**

### What is pointer jitter?

When SDH/SONET transmission bit rates are not synchronous, the time position of the payload containers must be adjusted in relation to the outgoing frames. This is done by incrementing or decrementing the pointer value by one unit. This shifts the payload signal by 8 or 24 bits, corresponding to a phase hit of 8 or 24 UI.

The output clock must be smoothed in a similar way to the stuffing process. In this case, though, much larger phase hits must be smoothed out much less frequently. The residual jitter has larger amplitudes and lower frequency components than stuffing jitter. Measurement of combined jitter (pointer and mapping jitter) uses defined pointer sequences to stimulate pointer jitter at the SDH/SONET input of a demultiplexer.

The following sample pointer sequences for the AU/STS level (87-3 pattern) are from ITU-T Recommendation G.783, ANSI 1.105.03 and Bellcore GR-253.

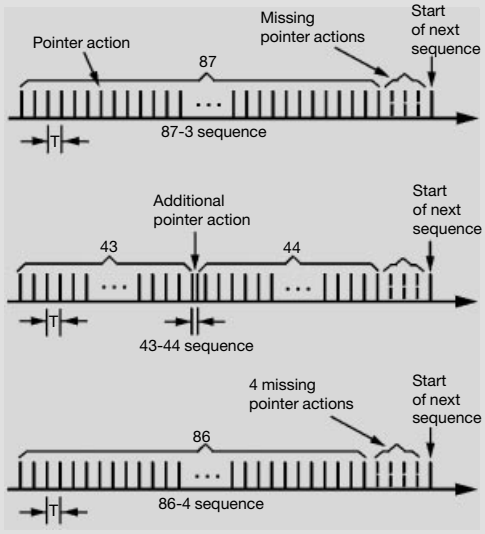



**Fig. 16: Examples of periodic pointer test sequences**

In these sequences, missing, double and inverse pointer actions are used. Based on experience, these sequences have been identified as the worst case scenarios and standardized as test cases.

## 3.5 Combined jitter

Differences in the clock signals in two networks or between network elements are compensated for by pointer movements in the synchronous signal (see also section 4.5). The pointer jumps correspond to 8 or 24 bytes, depending on the mapping. When the tributary signal is unpacked at the receiver, these pointer actions are still present in the form of phase hits. They are smoothed out using a PLL circuit. The residual phase modulation is called pointer jitter. The unpacked signal also includes mapping jitter in addition to pointer jitter, so it is always the sum of these two effects, i.e. the combined jitter, that is measured.

**Combined jitter** *(directly measurable)*
**=**
**Mapping jitter** *(directly measurable)*
**+**
**Pointer jitter** *(mostly not directly measurable)*

| G.783<br>GR-253<br>ETS 300 417-1-1 | Max. jitter [$UI_{pp}$] | Highpass cutoff | Lowpass cutoff |
|---|---|---|---|
| DS1 | 1.3 ... 1.9<br>0.1 | 10 Hz<br>8 kHz | 40 kHz<br>40 kHz |
| DS3 | 1.3<br>0.1 | 10 Hz<br>30 kHz | 400 kHz<br>400 kHz |
| 2 Mbit/s | 0.4<br>0.075 | 20 Hz<br>18 kHz | 100 kHz<br>100 kHz |
| 34 Mbit/s | 0.4<br>0.075 | 100 Hz<br>10 kHz | 800 kHz<br>800 kHz |
| 140 Mbit/s | 0.4 ... 0.75<br>0.075 | 200 Hz<br>10 kHz | 3500 kHz<br>3500 kHz |

**Table 3: Limits for combined jitter**

### 3.5.1 Test principle

The ANT-20 transmits a defined test signal to the network or network element. To assure that jitter is not caused by uncontrolled pointer movements, the test set and the network element are synchronized to the same reference clock (Fig. 17).

The network or network element is stressed by simulating the pointer sequences defined in the various standards (see Fig. 16, for example). The effects of these pointer sequences on the tributary output jitter are analyzed by the test set. The maximum values from Table 3 may not be violated. A 5 minute test interval is recommended.

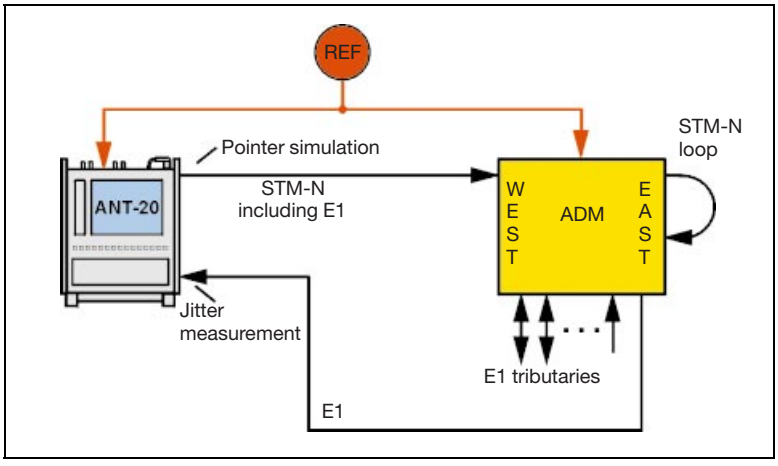



**Fig. 17: Determining the combined jitter**

### 3.5.2 Outputting the test results

It is the peak-to-peak values that are relevant when measuring combined jitter. The results are output like they were in section 3.1 “Measuring the output jitter”.

### 3.5.3 Further application: Automatic O.172 conformance suite for pointer sequences

To make certain that signals are transmitted error-free even when confronted with “worst case” pointer scenarios, some characteristic pointer sequences are tested. For example, for 140 Mbit/s there are seven different pointer sequences (five for DS1). These numbers are doubled in conjunction with the two action directions (“increment” and “decrement”).

Sequential testing of all of these cases manually would take a lot of time, and it would not be very effective. However, the built-in “CATS Test Sequencer” can automate this measurement. There is a predefined test sequence, which is oriented towards the procedure stipulated in ITU-T Rec. O.172 (Fig. 18).

**Explanation of the blocks:**

- *Initialization phase (INI):* Before each pointer sequence, an initialization sequence is transmitted to assure that the buffer in the pointer processor is at a defined starting position. This generally entails a sufficient number of pointer movements in the same direction as the test sequence.
- *Cool Down Phase:* An interval during which settling operations of the “desynchronizer” can be terminated.
- *Sequence n:* Setting for the respective pointer sequence (“max” = maximum number of pointer sequences)
- *Bandwidth f1 – f2 (f3 – f4):* The measurement should be performed with the two specified weighting filters (see also section 6, “Weighting filters”)

This is the basic procedure, but other variants are possible, e. g. including tests with different “tributary offsets”. Using the “CATS Test Sequencer”, you can develop different scenarios – without major programming expense – which are tailored to a given DUT.

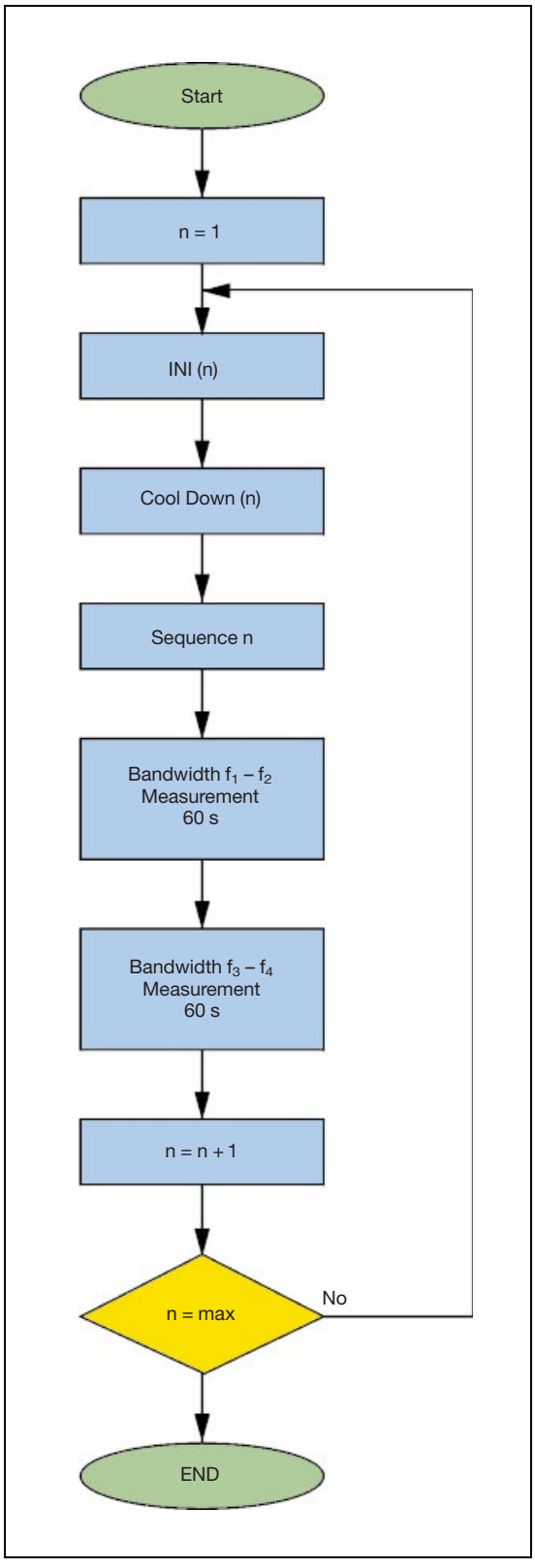



**Fig. 18: Flowchart for an automated pointer sequence**

**Important terminology**

**Primary Reference Clock (PRC)**
Frequency standard that provides a reference frequency for network synchronization as defined by various standards (e.g. long-term stability of $10^{-11}$ as per ITU-T Rec. G.811).

**Primary Reference Source (PRS)**
Frequency standard with long-term stability of $10^{-11}$ as per ANSI T1.101.

**Stratum Level:**
ANSI classifies the clock sources in synchronization networks into four quality levels. Stratum level 1 is the highest level and corresponds to the primary reference source (PRC).

**Synchronization Supply Unit (SSU)**
This unit includes functions for selecting the reference frequency and for further processing and distribution of this signal to the individual network elements. The SSU provides an improvement in the clock quality after passing through a longer synchronization chain. The SSU types are to some extent equivalent to Stratum Level 2 and 3.

**TNC (Transit Node Clock), LNC (Local Node Clock)**
These are different quality stages for SSUs. TNCs have better clock quality. In the newer ITU-T Recommendations, TNC is designated as SSU-A and LNC as SSU-B.

**BITS (Building Integrated Timing Source)**
A term from the ANSI norm. BITS has similar functions to SSU.

**UTC (Coordinated Universal Time)**
Time scale maintained by the "Bureau International des Poids et Mesures" (BIPM) and the "International Earth Rotation Service" (IERS). This time scale forms the basis for coordinating the distribution of time signals and standard frequencies.

**Global Positioning System (GPS)**
A global navigation system using radio satellites. The satellites are equipped with cesium and rubidium standard oscillators that are controlled from terrestrial stations. The extremely accurate clock signal transmitted by the system can be used to synchronize a primary reference clock.

# 4 Synchronization

Synchronization involves keeping different procedures on the same clock. In terms of synchronous networks (SDH/SONET), this means that all network elements must be oriented towards a single clock. In SDH and SONET, higher bit rates and synchronization are the major advances compared to older transmission technologies. This is the only way to assure uniform standardization at all hierarchy levels and represents a major challenge for system manufacturers and network operators.

## 4.1 Synchronization network architecture

A special synchronization network is set up to assure that all of the elements in the communications network are synchronous. The network is hierarchically distributed (Fig. 19).

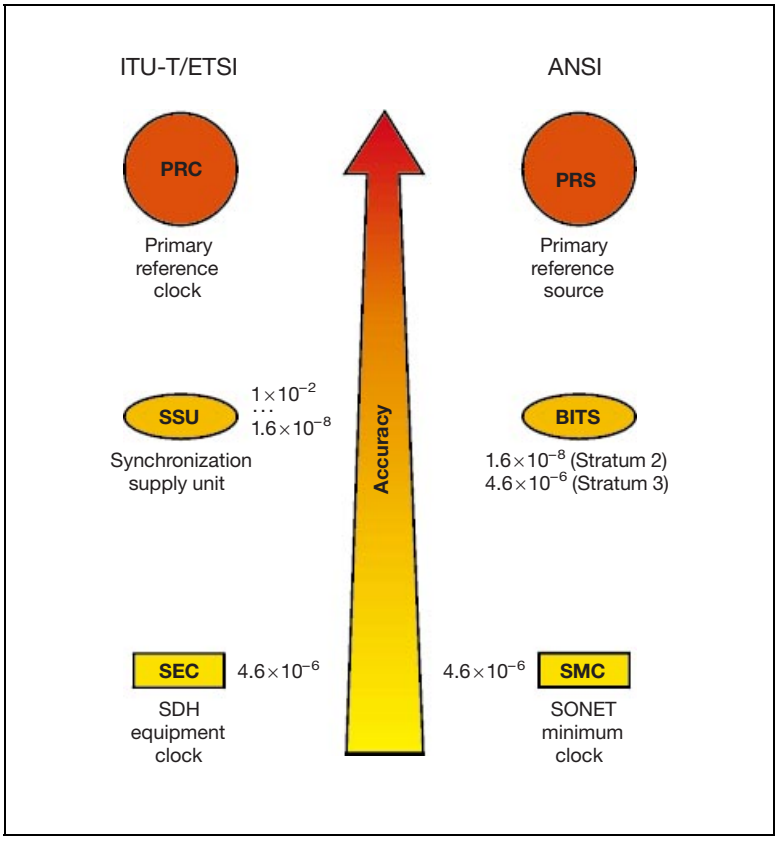



**Fig. 19: Clock hierarchies as per ETSI/ITU-T and ANSI**

A primary reference clock (PRC) controls the secondary clocks for the network nodes (SSU) and network elements (SEC). In contrast, only the exchange nodes are synchronized in PDH networks.

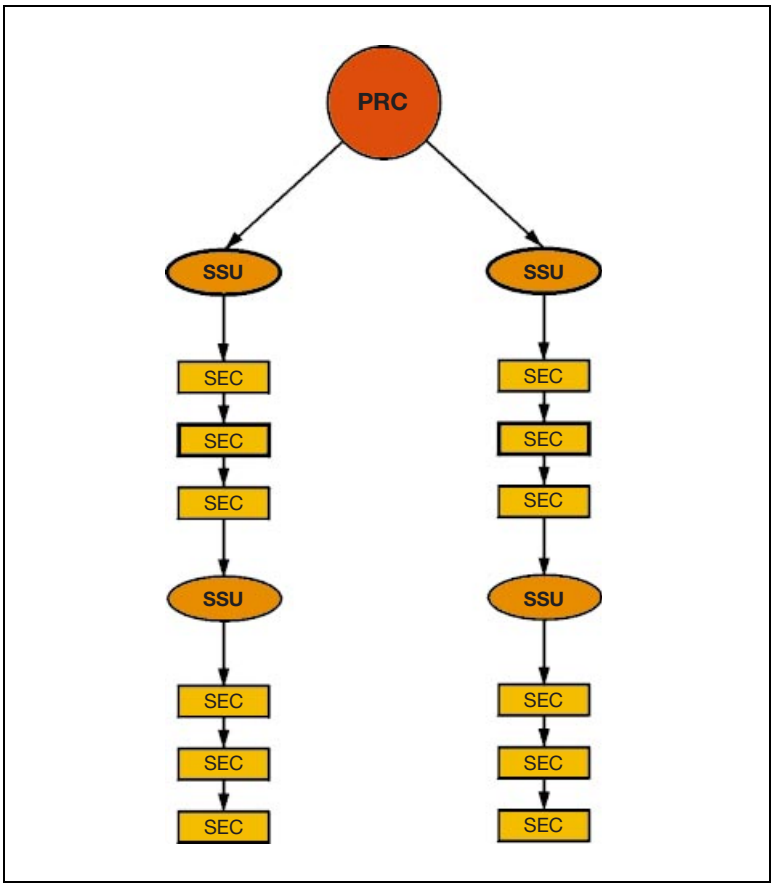



**Fig. 20: Sample synchronization chain**

This type of synchronization signal distribution is also referred to as master/slave synchronization. The actual synchronization may take place via a separate, exclusive sub-network, or the communications signals themselves may be utilized. Ring structures are also possible.

Under normal conditions, the reference signal from the PRC will be passed on by the next synchronization element in the chain. The outgoing clock signal is synchronized to the incoming signal to conform with various standards (e. g. ITU-T Recommendation G.812, 813). A PRC generates the master clock for the entire network or a sub-network, and all clocks are traceable to the PRC.

A PRC is usually implemented with a cesium oscillator and is based on timing standards such as LORAN C or GPS. The oscillator assures short-term stability and the radio signal long-term stability. It is important to make certain that UTC (Universal Coordinated Time) is maintained. SSUs are components that guarantee that timing is supplied to local components, whereas SECs are integrated into NEs.

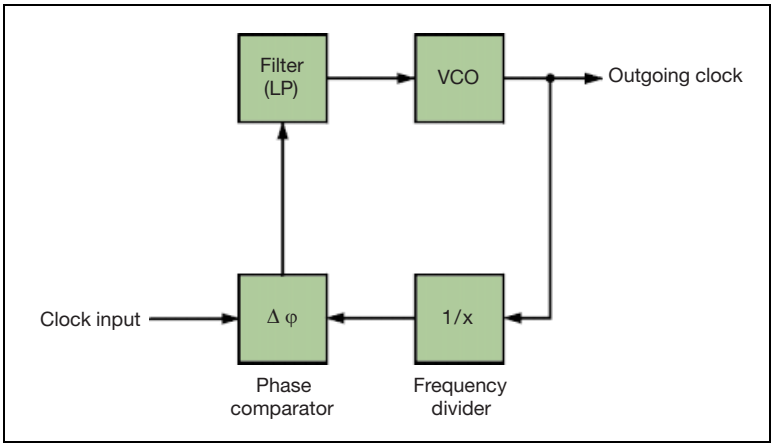



**Fig. 21: Basic principle of a phase locked loop (PLL)**

## 4.2 How does clock regeneration work?

Clock regeneration in SSUs (BITS) and SECs is generally handled using phase locked loops (PLL) (Fig. 21).

The control circuit of a PLL basically comprises a phase comparator, a narrow-band filter and a voltage-controlled oscillator (VCO). This circuit is used to “pull” the output clock to the reference clock. SSUs are designed as clock regenerators, so the filters generally have narrower bandwidths than those in the SECs built into NEs. The regenerated clock is therefore of higher quality. Of course, the accuracy of such regenerators is limited. They also introduce degradations due to intrinsic characteristics. As a result, the number of synchronization units in a chain must be limited.

ITU-T G.803 and ETSI 300 462 specify that the longest chain originating from a PRC must not exceed 10 SSUs, with not more than 20 SECs between two SSUs. The total number of SECs in a chain should not exceed 60.

## 4.3 Clock derivation in network elements

A network element can be synchronized using different clock sources:

- Clock input (T3) for an external clock source. This is ideally a PRC or an SSU interconnected between clock output (T4) and clock input (T3).
- Synchronous signal inputs (“aggregate” in ADMs) with clock derivation from the data signal.
- Tributary data inputs

If all the incoming (higher “quality”) clock signals fail or are unsuitable for synchronization, the affected unit switches to holdover mode. In this situation, an attempt is made to maintain the last correctly received signal as precisely as possible. To be able to do this, the frequency compensation values for the last 36 hours are stored along with the associated oscillator temperature. These data can be used to control the oscillator, achieving a ten- to hundred-fold improvement in stability compared with a free-running oscillator. Holdover mode must be capable of fulfilling certain phase conditions even over longer periods of time (e. g. several days).

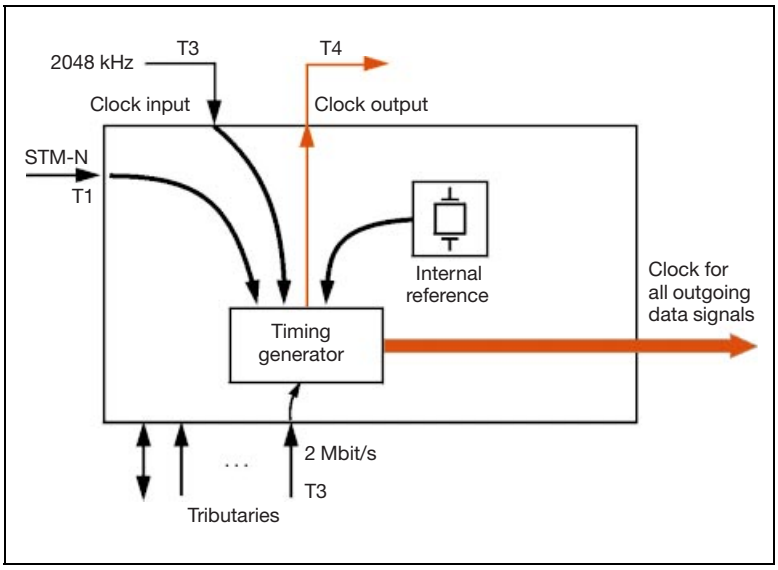



**Fig. 22: The different clock inputs of a network element**

**All of the outgoing data signals are synchronized to the selected clock source**

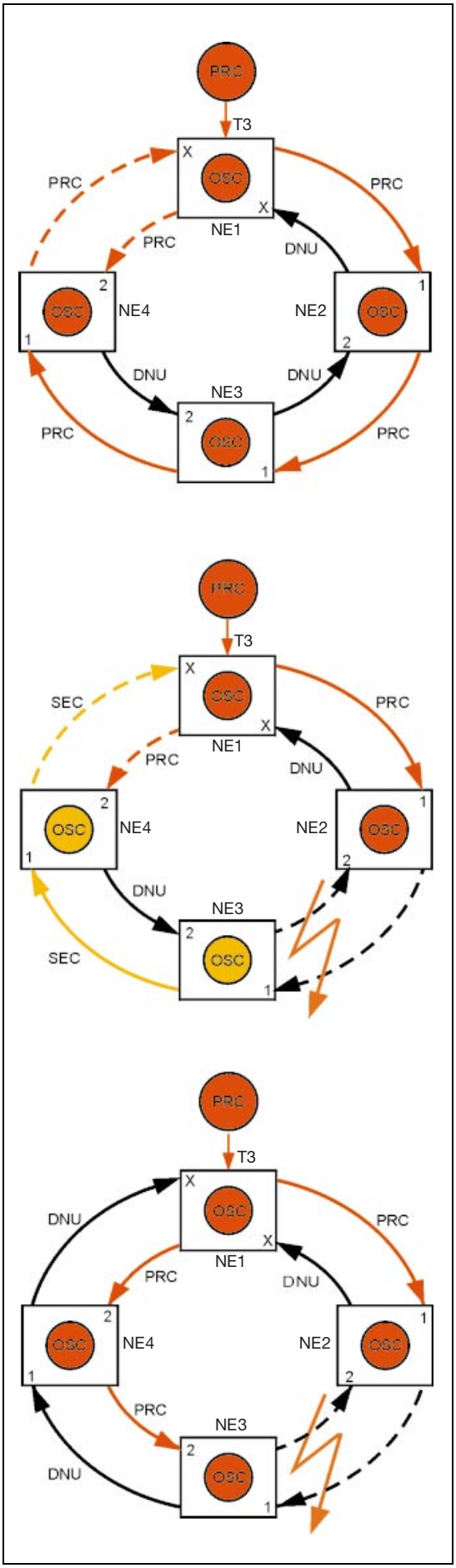
## 4.4 Usage of timing markers

“Timing markers” or “Synchronization status messages” offer one way to designate a signal in terms of its clock quality. The S1 byte of the SDH or SONET overhead is used for this purpose. Timing markers also play an important role in managing clock distribution. When properly used, spare paths for clock distribution can be provided during impairments to assure the clock quality within a network. “Priority tables” are used to specify what clock the network elements should choose when multiple clocks are available. To enable the network element to make a decision on clock selection, it is informed via the S1 bytes of the (data) signals which clock is suitable for synchronization purposes (Table 4).

In the ideal case, all of the timing markers in the clock flow direction correspond to the G.811 quality level. To prevent clock loops in which two network elements attempt to synchronize to one another, the timing marker “Don’t Use for Synchronization” is always inserted in the opposite direction of clock flow. If a network element does not receive a usable clock signal from any of the possible inputs (data, T3), then it uses its own internal clock source (“Holdover mode”).

**Table 4: Codes for clock quality**

| | **Synchronization Quality Level Description** | |
|---|---|---|
| **S1 bits (b5-b8)** | **SDH** | **SONET** |
| 0000 | Quality unknown (Existing Sync. Network) | Synchronized Traceability unknown |
| 0001 | Reserved | Stratum 1 Traceable |
| 0010 | G.811 (PRC) | — |
| 0011 | Reserved | — |
| 0100 | G.812 SSU-A | Transit Node Clock Traceable |
| 0101 | Reserved | — |
| 0110 | Reserved | — |
| 0111 | Reserved | Stratum 2 Traceable |
| 1000 | G.812 SSU-B | — |
| 1001 | Reserved | — |
| 1010 | Reserved | Stratum 3 Traceable |
| 1011 | Synchronous Equipment Timing Source (SETS) | — |
| 1100 | Reserved | SONET Minimum Clock Traceable |
| 1101 | Reserved | Stratum 3E Traceable |
| 1110 | Reserved | Provisionable by the Network Operator |
| 1111 | Don’t Use for Synchronization | Don’t Use for Synchronization |




## Example: Ring synchronization Switch-over in case of a fault

Figs. 23a to 23c give a simple example of ring synchronization using four network elements and a PRC clock source:

- Configuration of network elements for clock distribution
- Clock distribution behavior when a fault occurs

During normal operation, the complete ring is clocked by the PRC, which is directly connected to NE 1 (clock input T3). This NE cannot derive a clock from the data inputs and is not configured initially as a clock port. This prevents possible clock loops.

The other three network elements derive the clock from the incoming data signals. The best clock source is always used (here, PRC). The output signals have this clock quality, so PRC is indicated in the S1 byte. To avoid clock loops, “Don’t Use for Synchronization” (DNU) is indicated in the S1 byte in the opposite direction.

At NE 4, PRCs are present at both data ports. In this case according to the clock derivation table determining the priority in case of identical clock priority, the clock from NE 3 is used.

## What happens to the ring in case of a fault (e. g. between NE 2 and NE 3)?

In this case, NE 3 no longer receives a valid synchronization signal from NE 2, so it operates in holdover mode (Fig. 22b) since an alternative clock source is not yet available. This is also indicated in the S1 byte (“SEC”) towards NE 4. NE 4 now receives a signal with PRC quality from NE 1 in the reverse direction. According to the clock derivation table, NE 4 takes the synchronization clock from the reverse direction (NE 1). The same applies to NE 3, which uses the clock from NE 4 from the reverse direction (Fig. 22c). Despite the disruption, all of network elements still use the PRC clock.

**Fig. 23: Synchronization in a ring with four network elements and a PRC clock source**

## 4.5 Clock compensation using pointer actions

Pointer technology is very sophisticated and is one of the fundamental features of SDH/SONET systems. Pointers are used to flexibly identify individual virtual containers in the payload of the synchronous transport module (Fig. 24).

Due to the complexity of pointers, not all of the details can be covered here. If you need more information, refer to a reference text such as *Kiefer, R.: Test solutions for digital networks (Hüthig 1997)*.

Pointer technology is used to process possible phase differences due to a clock offset or wander between, say, the incoming VC-4 (STS-3c) and the outgoing STM-N (STS-N) frames. This situation occurs when a network element is out of synchronization, i. e. in holdover mode.

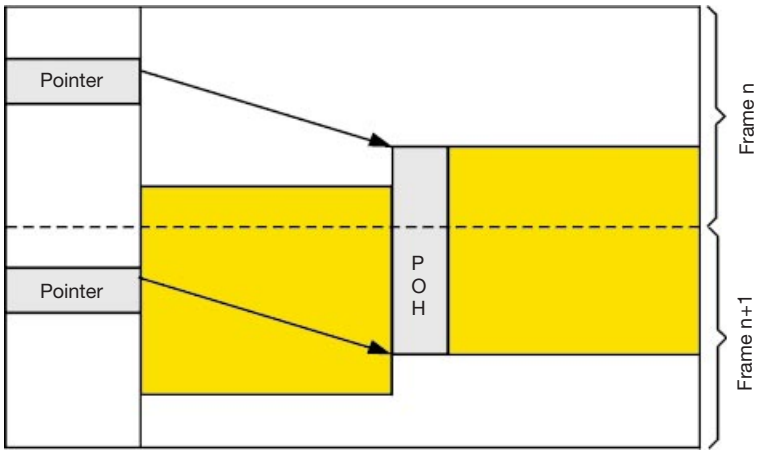



**Fig. 24: Pointers identify virtual containers in the payload of the STM-N signal**

**Pointer increment (INC)**
If the incoming data signal is slower than the reference clock ("Offset –"), then too little data arrives for the outgoing transport signal (Fig. 25). The payload is "shifted forward" virtually and the pointer value increased. The bytes freed up in this process are replaced with stuffing bytes ("positive pointer stuffing"). The effective bit rate for the user data is artificially decreased in this manner.

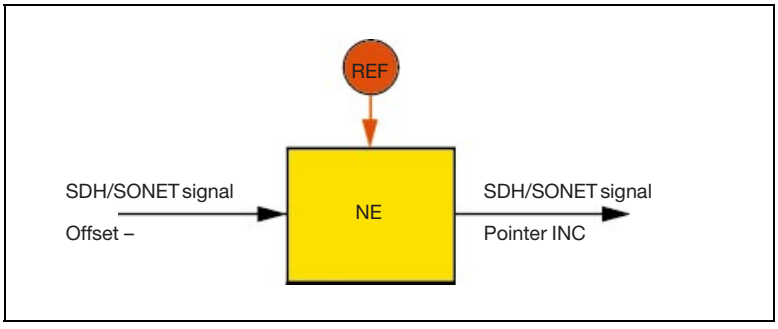



**Fig. 25: If the incoming data signal is slower than the reference clock ("Offset –"), then the pointer is incremented.**

**Pointer decrement (DEC)**
If the incoming data signal is faster than the reference clock ("Offset +"), then too much data arrives for the outgoing transport signal (Fig. 26). The payload is "shifted backward" virtually and the pointer value decreased. The missing bytes are inserted into the SOH overhead ("negative pointer stuffing").

In the worst case in which the clock generator of a network element (SEC) is operating at the maximum allowable frequency error of $4.6 \times 10^{-6}$, then about 30 pointer actions per second are required for adaptation. This value is far below the maximum pointer frequency of 2000 pointer actions per second. Extreme offsets result in overflow of the buffer in the pointer process. The pointer value then has to be reset with NDF (New Data Flag), and parts of the payload are lost definitively.

Due to the byte structure of SDH signals, the pointer corrections always take place as "jumps" of one or three bytes. If PDH signals are transported, then pointer events cause "pointer" jitter to appear on PDH outputs (for more information on pointer jitter, see pp. 12 – 13).

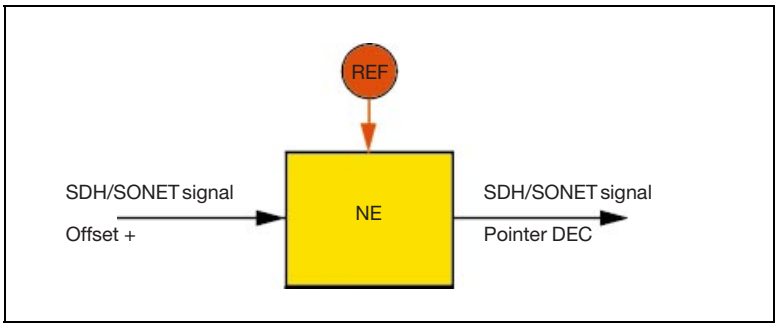



**Fig. 26: If the incoming data signal is faster than the reference clock ("Offset +"), then the pointer is decremented.**

## 4.6 Test applications

The clock quality has a basic influence on the overall network quality. In SDH/SONET network elements, the clock derivation priority tables must be manually entered when commissioning the network element. They determine the clock source used to synchronize the network element (see section 4.4). An incorrect entry (or simply forgetting to enter a value) means that the network element will operate in free-running mode with the internal clock source. In that case, it is not suitable for timing in the SDH network, and any clock difference that arises will be compensated using pointer actions. However, this results in increased output jitter at the PDH outputs. Pointer actions are particularly disruptive when transmitting PDH signals used to transport synchronization clocks.

To gain an initial impression of the network clock quality, we recommend performing a pointer analysis at the STM-N level at a protected monitor point.

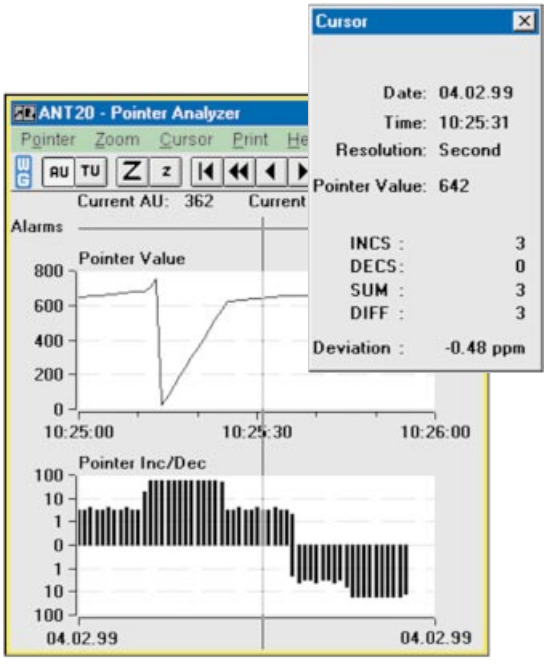



**Fig. 27: Trace of pointer activity over a one minute interval. The ANT-20's pointer window lets you simultaneously observe AU and TU pointer values, with the absolute value displayed in numerical and graphical formats. Pointer increments and decrements are shown separately. The frequency offset associated with the respective pointer operation is automatically computed and displayed.**

### 4.6.1 Pointer analysis

An increased number of pointer actions in the same direction indicates a non-synchronous clock source in the network. If such pointer actions commonly occur in the network, it is necessary to determine why. One way to do this involves tracing the transmission segments step-by-step. There are no international recommendations on the maximum number of pointer actions per day. In practice, it is common to encounter from 1 to 50 pointer actions per day with good clock quality. It is important that these pointer actions are distributed over the day. Depending on the manufacturer, double pointers (two pointers per second) can also be encountered. Since a long-term measurement is necessary, you should make sure to measure over an interval of at least 24 hours.

In the ANT-20's Anomaly/Defect Analyzer, pointer adaptations (Pointer Justification Event = PJE) as well as NDF events (New Data Flag = NDF) are displayed. If NDF events are measured, then the clock problems are so severe that parts of the payload were lost.

### 4.6.2 Monitoring the "timing marker" S1

With the ANT-20's Overhead Analysis tool, you have access to all SDH/SONET overhead bytes, including the timing maker S1. The content of the S1 byte is displayed in plain-text (Fig. 28).

In long-term monitoring mode, it makes sense to record any changes in the S1 byte (overhead byte capture function). This is the way to record a transition in the S1 byte from "G.811" to "Quality unknown" with a time-stamp, which can be caused by failure of the PRC, for example.

Monitoring the timing marker gives an indication of proper configuration of the clock derivation tables and can be useful when attempting to identify clock problems. However, accurate assessment of clock quality is possible only through wander analysis (see section 5 for details).

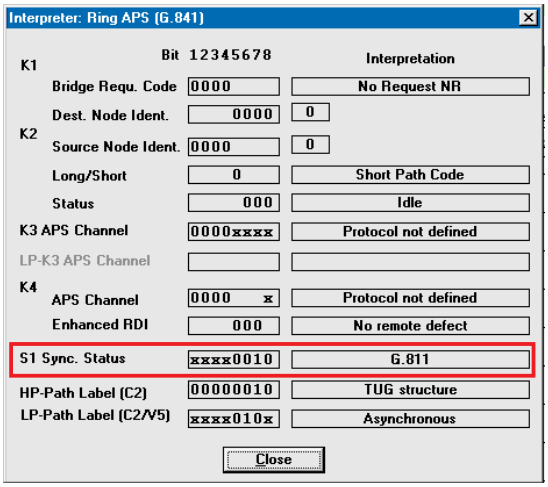



**Fig. 28: The content of the analyzed S1 bytes is shown in plain-text.**

# 5 Wander applications

## 5.1 Wander measurement

Good network synchronization is a prerequisite for network availability. We recommend monitoring the wander parameters during installation, at routine intervals during operation and after changes in the network topology. Don't wait until customers complain!

### 5.1.1 Test principles

A clock reference is a basic prerequisite for measurements. It can be an external reference source or the next higher clock signal in the network's synchronization chain (absolute or relative measurement).

The same input jacks are used for the signal under test as with other ANT-20 measurements (e.g. anomaly/defect analysis or performance and pointer tests). This means that wander measurements can be performed in parallel to these measurements on all relevant interfaces up to STM-16 and even on ATM signals. There is a separate jack for the reference clock, and it accepts clock signals at 1.5 MHz, 2 MHz and 10 MHz as well as data signals with bit rates of 1.5 Mbit and 2 Mbit/s.

The measurement results are TIE vs. time, and the TIE sampling rate can be matched to the application prior to measurement:

- 1/s for long-term measurements up to 99 days
- 30/s for standard wander acceptance measurements that comply with O.172 (e.g. 24 h)
- 300/s for precision analysis of the phase transient response (see section 5.2)

**Example 1:**
**Absolute measurement of clock quality**

In the scenario shown here, a small network operator obtains its clock from a larger network operator via a data line (STM-1 or PCM-30). Using an absolute measurement with respect to an external reference source, the quality of the clock signal can be checked.

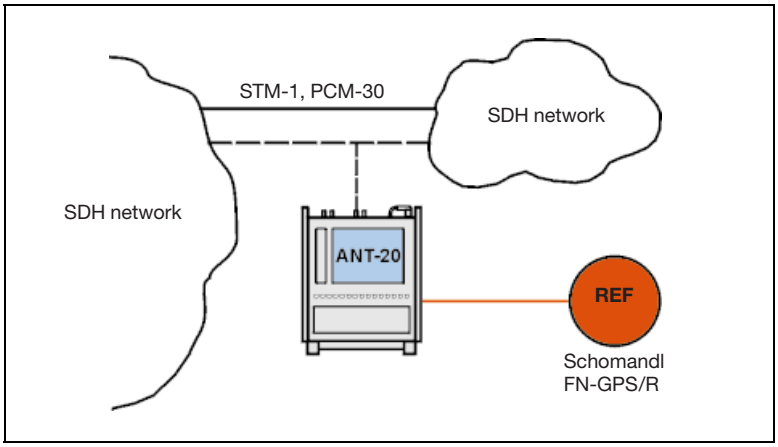
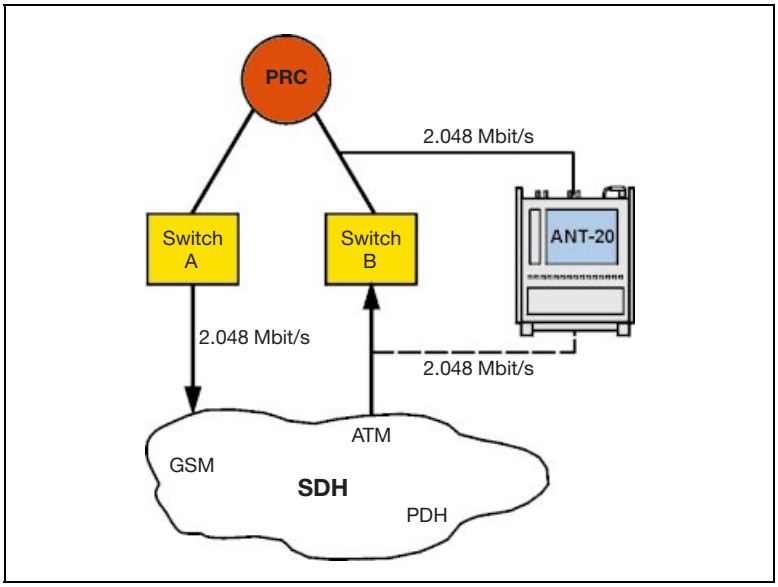



**Fig. 29: Clock quality measurement at network boundaries (absolute measurement)**

**Example 2:**
**Relative measurement of clock quality**

In this example, relative measurement makes the best sense: Two switches (A and B) are synchronized to a PRC. A signal path (e.g. 2 Mbit/s) is routed via different transport networks (SDH, PDH, etc.). Interfering factors such as delay fluctuations, mapping/pointer wander and oscillator noise can produce such great phase deviations that a frame slip occurs. Using a TIE or MTIE measurement, you can determine whether the phase deviations are within the specified limit of 18 µs/day (ITU-T G.822 and G.823).

**Fig. 30: Measurement on a signal routed via multiple networks (relative measurement)**



### 5.1.2 Displaying the test results

The TIE vs. time curve is shown in real time. Measurements and analyses can run concurrently in other ANT-20 windows. The current values for TIE and MTIE are shown numerically. MTIE is determined here as the difference between the maximum and minimum TIE values since the start of the measurement.

Using the built-in offline analysis software, more in-depth analysis can be performed, as will be further explored in section 5.2.

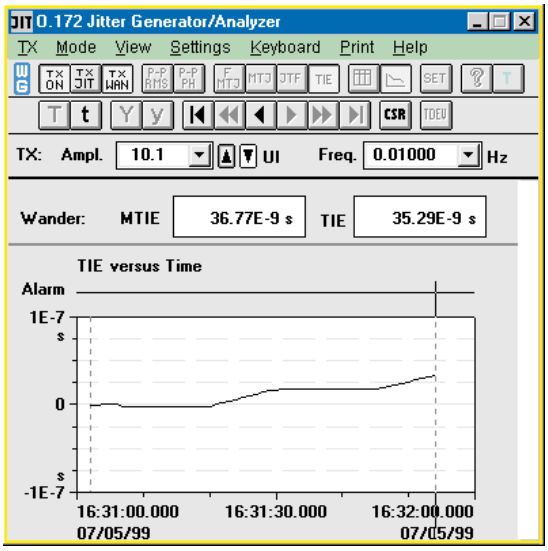



**Fig. 31: Graphical presentation of wander results. The current TIE and MTIE values are given numerically. The TIE vs. time curve is shown graphically.**

## Important wander measurement terminology

Wander measurements are very similar to jitter measurements. However, instead of using an internal reference clock generator as is customary in jitter measurement, an external reference clock with minimum intrinsic wander must be supplied since phase fluctuations down to nearly 0 Hz are measured.


**Fig. 32: Basic principle of wander measurement: Phase comparison between two clock signals**

In many SDH networks, clock information is distributed between network elements using the STM-N transmission signal. The test set must be capable of performing wander measurements using the signals on the optical or electrical interfaces.

**Time Interval Error (TIE):** The TIE value represents the time deviation of a clock signal under test relative to a reference source. The measurement is referred to an observation interval s (in seconds). It is usual to arbitrarily set the start of the interval to zero, i. e. TIE(0) = 0. TIE measurement is the basis for other calculations (MTIE, TDEV).

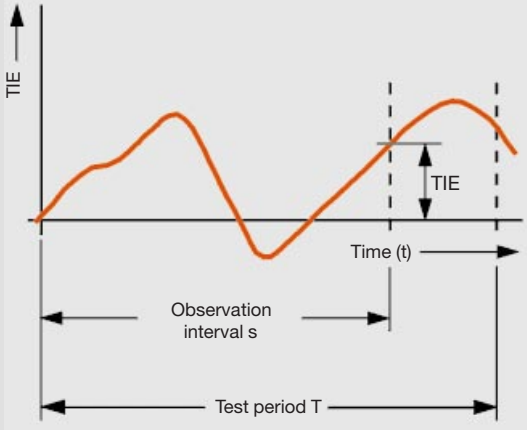



**Fig. 33: Determining the TIE value**

Unlike jitter results, which are given in UI (relative to the bit rate), TIE values are given as absolute values in seconds (or in ns). Modern test sets gather the phase values through digital sampling, and ITU-T G.813 requires at least 30 samples per second (for lowpass filtering with a 10 Hz cutoff frequency as per O.172). However, ANSI T1.101 requires higher sampling rates and a cutoff frequency of 100 Hz. ETS 300 462-3 defines a cutoff frequency of 0.1 Hz for very long observation intervals.

**MTIE (Maximum Time Interval Error):** MTIE is the maximum time interval error (peak-to-peak value) in the clock signal being measured (compared with a reference clock) that occurs within a specified observation interval s. In the simplest case measurement (instantaneous value detection), the starting point for the interval is fixed, and the interval is increased by increasing the measurement time. This already allows the relative frequency offset $\Delta f/f$ to be determined approximately by dividing the MTIE value for the interval s by the interval s itself, since:

$$\Delta f/f \cong \text{MTIE}(s)/s$$

**Example:**

MTIE (1s) = 12 µs
$\Rightarrow \Delta f/f = 12 \cdot 10^{-6}$ (12 ppm)

MTIE (10s) = 15 µs
$\Rightarrow \Delta f/f = 1.5 \cdot 10^{-6}$ (1.5 ppm)

**MTIE offline algorithm:** A more precise result is obtained using the complete algorithm specified in ITU-T G.810, ETS 300 462-1 and ANSI T1.101. Here, a variable observation interval s (Fig. 34) "travels" through the entire measurement time T with the maximum deviation being retained (MTIE value for the interval s).

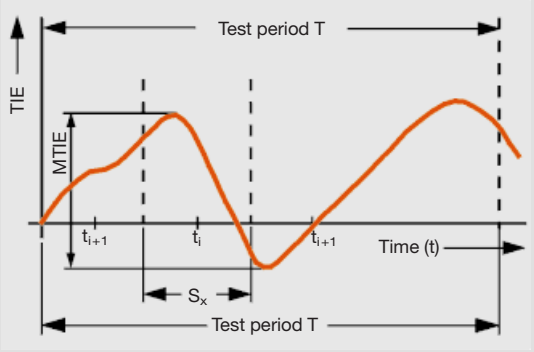



**Fig. 34: Determining the MTIE value**

Simplified MTIE algorithm:
- Observe all 1 s intervals.
- Determine the maximum time deviation within each observed 1 s interval (MTIE values for 1 s).
- Enter the highest value against the 1 s mark in the MTIE graph.
- Observe all 2 s intervals.
- Determine the maximum time deviation within each observed 2 s interval (MTIE values for 2 s).
- Enter the highest value against the 2 s mark in the MTIE graph.
- Repeat for other time intervals (3, 5, 8 s, etc.).

The MTIE calculation is suitable for detecting a frequency offset but does not give any information about the spectrum of the error signal.

### 5.1.3 Other applications

**Wander generation**
Wander simulation is a means of feeding selected wander frequencies to a device under test so its response can be checked with the ANT-20's analysis facilities. The ANT-20 can generate wander frequencies down to 10 µHz.

**Testing wander tolerance**
This test is basically like the MTJ test (section 3.2), except that wander is a long-term phenomenon. To check several wander frequencies and amplitudes, you need significantly more time than in a comparable MTJ test. Table 5 illustrates this problem.

| Wander frequency | Period |
|---|---|
| 10 µHz | 27.8 h |
| 1 mHz | 1000 s = 16.7 min |
| 1 Hz | 1 s |

**Table 5: Frequency and period correspondence for wander**

Even at low wander frequencies, you should let the measurement run for at least one full period.

Given the long test times, manual testing is obviously not practical. This measurement is implemented in the ANT-20 using the "CATS Test Sequencer" so that all wander frequencies can be automatically checked one after another.

## 5.2 Offline wander analysis

The MTIE/TDEV analysis software considerably extends the wander analysis capabilities described in the previous section.

### 5.2.1 Test principle

Offline wander analysis is based on TIE samples gathered during a wander measurement. Two file formats are accepted: The ANT-20's file format and the *.csv file format (compatible with MS Excel).

Using the recorded TIE samples, an MTIE/TDEV analysis can be performed to ETSI Recommendation ETS 300 462 (as per ITU-T G.810, G.811, G.812, G.813). The frequency offset and drift rate are also computed to ANSI T1.101 (see also p. 27).

You can install the MTIE/TDEV software on the ANT-20 or a separate PC. It computes the MTIE and TDEV curves with the specified algorithms. All tolerance masks are available for evaluation purposes that are required for qualifying synchronization elements (e.g. as per the ANSI, ETSI and ITU-T norms). To provide a quick overview, a "software LED" delivers a PASS/FAIL result. User-specific tolerance masks can also be programmed.

The built-in software simulator makes it easy to superimpose sinusoidal, linear or square-wave signals or even white noise to give a "virtual" TIE curve. They can also be evaluated using the software and compared with "real" measurement traces.

### 5.2.2 Displaying the test results

The offline analysis software has two presentation formats:

**TIE analyzer**
This mode lets you examine the recorded TIE samples in greater detail. Zoom functions make it easier to identify and analyze crucial time segments. Several TIE measurements can be loaded into the TIE analyzer and compared, e. g. several measurements on the same DUT (Fig. 35). The frequency offset and the drift rate are also displayed. The frequency offset can be eliminated (frequency-offset-compensated TIE display). The zoom function lets you pick a reasonable evaluation interval for MTIE/TDEV offline analysis.

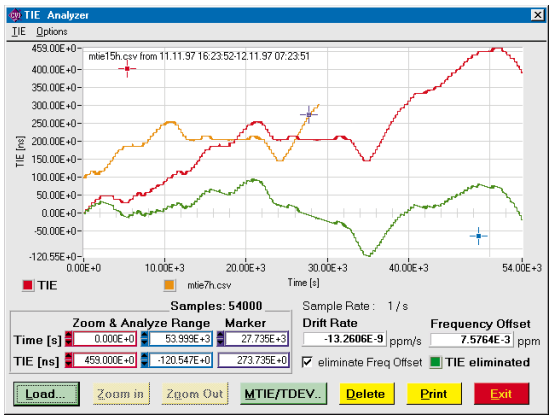



**Fig. 35: The TIE analyzer showing multiple TIE measurements**

**MTIE/TDEV window**
This mode lets you start the MTIE and the TDEV algorithm. Reasonable observation intervals within the overall measurement time are used for computation purposes, and the results for each interval are displayed as a point.
Various tolerance masks can be inserted which characterize the different quality levels (e. g. PRC level, SSU level).

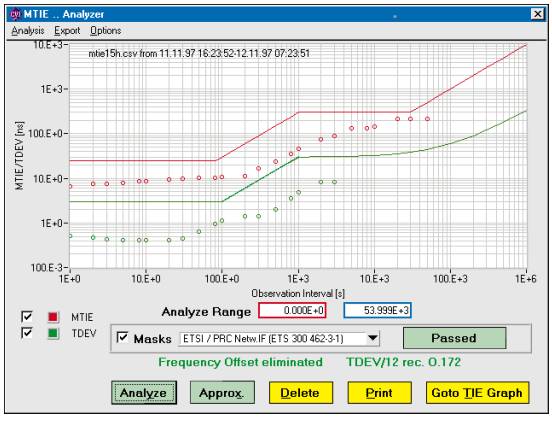



**Fig. 36: MTIE and TDEV analysis, shown here with tolerance mask (passed)**

### 5.2.3 Investigating the phase transient response

A wander measurement (TIE) is useful for checking the phase transient response. However, set the TIE sample rate to 300/s for a larger resolution so that any fast transients can be detected. The resolution achieved is 10 times higher than the figure specified in O.172. The offline analysis software allows you to investigate the phase transient response with even greater precision. You can use the 200 m function to precisely select and analyze the time segment.

Besides 24 hour acceptance tests “in compliance with O.172, PRC level” and long-term monitoring work in combination with a bit error rate test (BERT), investigation of phase transient response is particularly important. Phase transients arise at the outputs of synchronized clock generators due to interference to the reference signal, e. g. when the synchronization signal is interrupted or when switching between different synchronization sources. One distinguishes between short-term and long-term phase transient response.

**Short-term phase transient response**
This occurs when an impairment causes a switch-over to another reference source for which the same primary source is the basis (Fig. 37). After switch-over, the phase must settle down to the new synchronization source, which may last up to 15 s. A maximum clock deviation of 1000 ns is stipulated as the tolerance mask (see ITU-T Rec. G.813).

**Long-term phase transient response**
This occurs when the synchronization source is lost and the clock generator has to go into holdover mode. Since a frequency offset can last in this case over a longer time period, the phase deviation over time is basically unlimited. However, based on the maximum tolerable frequency error in holdover mode, there is a maximum slope of the phase deviation vs. time (Fig. 38).

The frequency offset of $4.6 \times 10^{-6}$ may not be exceeded by a SEC. The value is directly displayed in the analysis window.

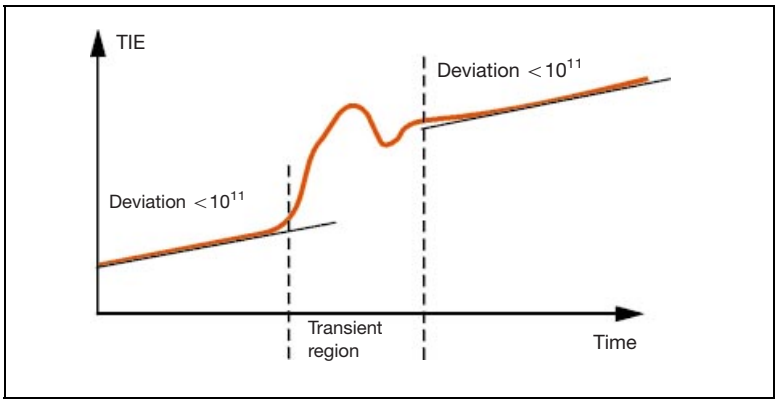



**Fig. 37: Short-term phase transient response**

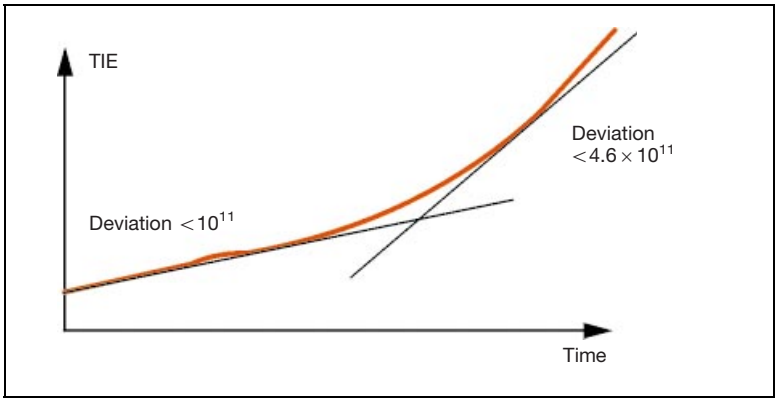



**Fig. 38: Long-term phase transient response (“holdover mode”)**

**TDEV (*Time Deviation*)**
The TDEV value is a measure of the phase error variation versus the integration time, i. e. a statistical value. It is calculated from the TIE samples. Put simply, the standard deviation $\sigma(s_i)$ is calculated for each point $s_i$ within a measurement time T for an interval s which "travels" through the entire measurement time (see under MTIE) (Fig. 39). The calculated values are averaged over T to obtain the TDEV value for the interval s. The interval s is then increased and the procedure repeated for the "new" value of s.

In contrast with the MTIE calculation, TDEV analysis provides information about the spectral content of the phase variation and the results can be interpreted as indicated in the diagram below:

Simplified TDEV algorithm:
- Observe all 1 s intervals.
- Determine the standard deviation s within each interval.
- Average all values of s over the measurement time T (this gives the TDEV value for 1 second).
- Enter this value against the 1 s mark in the TDEV graph.
- Observe all 2 s intervals.
- Determine the standard deviation s within each interval.
- Average all values of s over T (TDEV for 2 s).
- Enter this value against the 2 s mark in the TDEV graph.
- Repeat for other time intervals (3, 5, 8 s, etc.).

The TDEV calculation can be considered as a traveling software filter. The TDEV values for the intervals $s_x$ are obtained by "digital filtering" using a bandpass filter with center frequency $0.42/s_x$ followed by calculation of the RMS value.

**TVAR (*Time Variance*)**
Represents mathematically the square of the TDEV.

**ADEV (*Allan Deviation*),**
**MADEV (*Modified Allan Deviation*)**
The ADEV and MADEV calculations are comparable with the TDEV calculation (they are also mathematically related). ADEV and MADEV are not used as often as TDEV but are sometimes useful for analysis, since they give more information about the nature of the impairments.

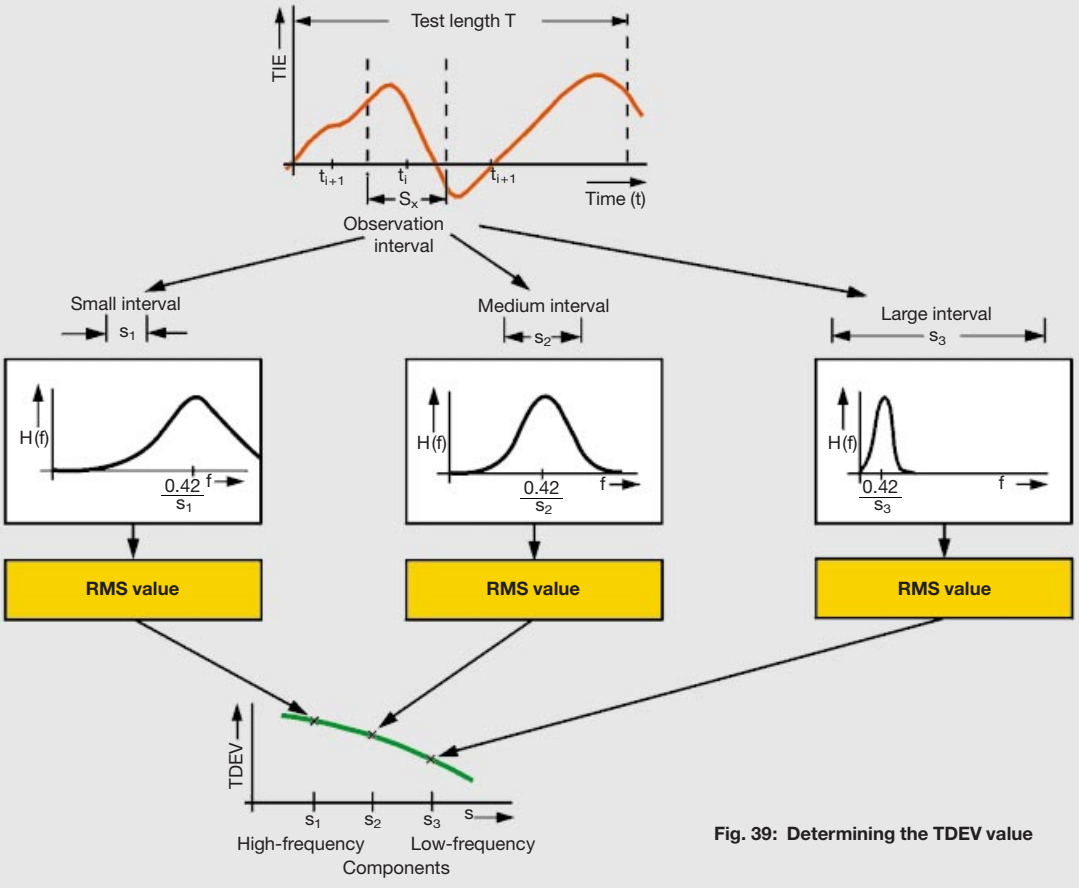



**Fig. 39: Determining the TDEV value**

### Interpreting the MTIE, TDEV, ADEV and MADEV curves

ADEV, MADEV and TDEV may yield different results depending on the type of interference signal (see Table 2, p. 28). As well as the obvious effects due to frequency offset and drift, the typical noise processes encountered in oscillators are also listed.

As the table shows, the MTIE calculation is the only method described that can detect the important (and frequently occurring) case of frequency offset. On the other hand, the TDEV calculation gives information about frequency drift or oscillator noise. If, for example, the slope of the TDEV curve corresponds to the square root of s, this indicates phase modulation with white noise.

Buffers are used in digital switches, synchronous cross-connects and add-drop multiplexers to compensate for the frequency variations caused by pointer actions. The MTIE value is useful for configuring the buffer, i.e. the buffer is dimensioned according to the specified limit value for MTIE. If this value is not exceeded it can be safely assumed that no buffer overflows will occur and hence frame slips will be absent.

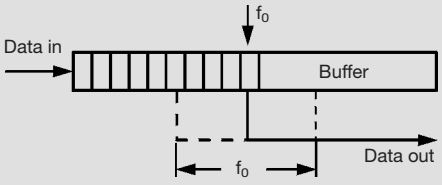



**Fig. 40: Buffers are used to compensate for frequency fluctuations**

The TDEV, ADEV and MADEV curves cannot be used to dimension the buffers, but they are useful for assessing oscillator performance. ETSI 300 462-3 specifies MTIE and TDEV masks for all synchronization elements (PRC, SEC, SSU, PDH). These indicate the maximum MTIE or TDEV value for each observation interval. To summarize:

- ***MTIE is a measure of the long-term stability of a clock signal,***
- ***TDEV a measure of the short-term stability.***

### Frequency offset and frequency drift rate

Besides specifying the phase transient response (TIE) for switch-over of a clock source to holdover mode, the standards also stipulate maximum values for the "initial fractional frequency offset" and the "frequency drift rate". The values are determined using special algorithms from ANSI T1.101 (see Table 7, p. 28).

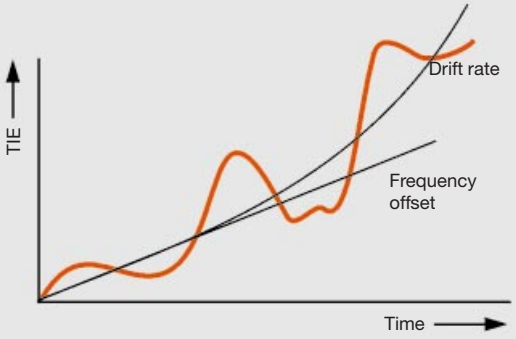



**Fig. 41: Influence of the drift rate and frequency offset on TIE (Time Interval Error)**

### MRTIE (*Maximum Relative Time Interval Errors*)

If during wander analysis the reference is not available, e.g. due to spatial separation, the MTIE analysis can have a frequency offset superimposed on it. It is a function of the clock difference between the signal and the local reference used for measurement. In the RMTIE measurement, the frequency offset is subtracted from the result so that the true wander is displayed.

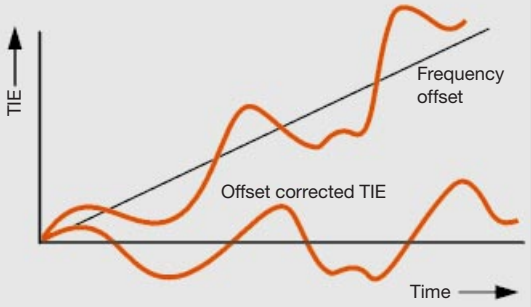



**Fig. 42: In the RMTIE measurement, the frequency offset is subtracted from the result**

| Process | Slope of | | | | Possible causes |
|---|---|---|---|---|---|
| | MTIE | TDEV | ADEV | MDEV | |
| Frequency offset | s | – | – | – | Clock not from PRS |
| Frequency drift | – | $s^2$ | s | s | Delay variations due to temperature changes |
| White noise phase modulation (WPM) | – | $s^{-1/2}$ | $s^{-1}$ | $s^{-3/2}$ | Typical parasitic noise processes in different types of oscillators |
| Flicker Phase Modulation (FPM) | – | $s^{-0}$ | $s^{-1}$ | $s^{-1}$ | |
| White noise frequency modulation (WFM) | – | $s^{1/2}$ | $s^{-1/2}$ | $s^{-1/2}$ | |
| Flicker frequency modulation (FFM) | – | s | $s^0$ | $s^0$ | |
| Random walk frequency modulaton (RWFM) | – | $s^{3/2}$ | $s^{1/2}$ | $s^{1/2}$ | |

**Table 6: Interpretation of MTIE, TDEV, ADEV and MDEV curves to ETSI 300 462-1**

| | Stratum 3 | Stratum 3E |
|---|---|---|
| Initial frequency offset | 0.05 ppm | 0.001 ppm |
| Frequency drift rate | $4.63 \times 10^{-7}$ ppm/sec | $1.16 \times 10^{-8}$ ppm/sec |
| Fractional frequency offset due to temp. variations | 0.3 ppm | 0.01 ppm |

**Table 7: Limits for the Stratum-3/3E clock source as per ANSI T1.101**

# 6 Jitter and wander test equipment

**Basics of jitter measurement** A jitter test set is basically made up from the following items:
- Pattern clock converter
- Reference clock generator
- Phase meter
- Weighting filters
- Peak value detector (with possible RMS determination).

The pattern clock converter generates the clock signal from the digital signal, with all its attendant phase deviations. This clock signal is then compared to the reference clock in the phase meter.

The reference clock generator provides a phase reference by slowly tracking the jittered input clock with the aid of a phase locked loop (PLL). The PLL has a lowpass filter with a cutoff frequency in the range of 1 Hz (ANT-20: 0.1 Hz) so that high-frequency jitter components are filtered out. The PLL bandwidth also determines the lower limit frequency for jitter measurement, i.e. components below this frequency are not detected.
The voltage fluctuations at the output of the phase meter are proportional to the phase fluctuations, i. e. the output signal corresponds to the jitter vs. time curve. Standardized weighting filters

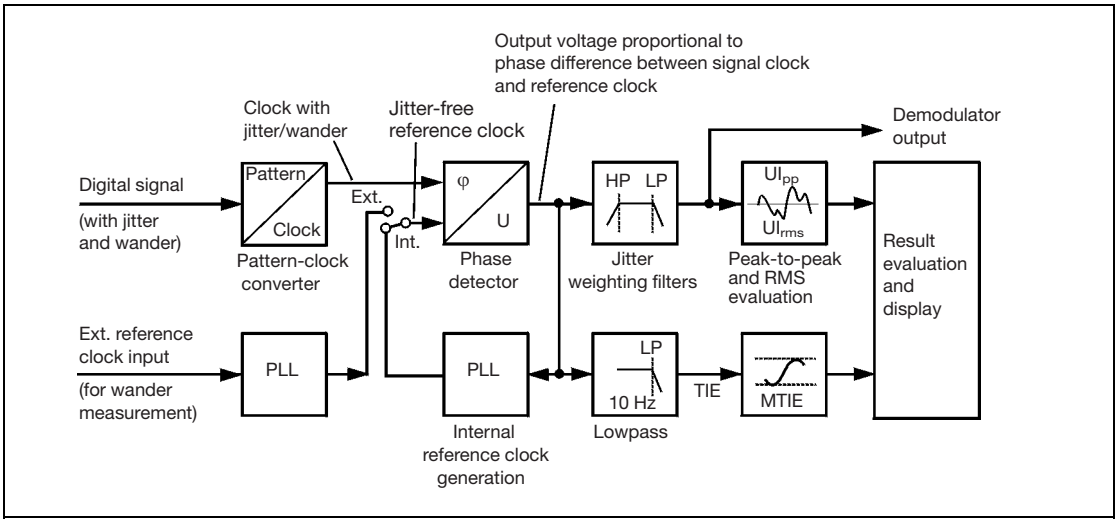
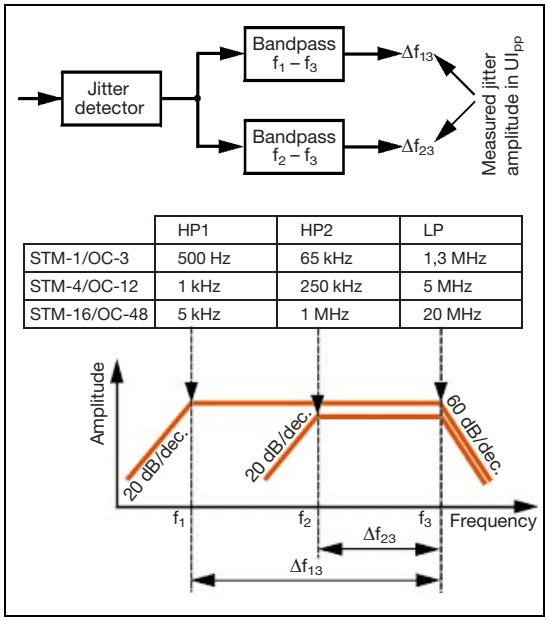



**Fig. 43: Block diagram of a jitter/wander analyzer**

connected after this (see below under “Jitter weighting”) limit the frequency spectrum of the jitter signal. The positive and negative peak values of the filtered signal are measured (peak-to-peak evaluation) and displayed as the jitter result (in $UI_{pp}$ or alternatively in RMS). The filtered signal is available at a demodulator output for further external processing. Further time- and frequency-domain analysis of the jitter is thus possible, e. g. using an oscilloscope, a selective level meter or a spectrum analyzer.

**Jitter weighting**

Combinations of high-pass and low-pass filters weight the detected jitter signal with regard to its spectral content. The filter combinations for the various transmission interfaces are specified in the relevant standards (see Appendix, Table 3: “Standards for jitter and wander”). Jitter analyzers are therefore equipped with an appropriate selection of highpass and lowpass filters. By selecting certain frequency ranges from the jitter spectrum, conclusions can be drawn regarding the frequencies causing the observed problems.




| | HP1 | HP2 | LP |
|---|---|---|---|
| STM-1/OC-3 | 500 Hz | 65 kHz | 1,3 MHz |
| STM-4/OC-12 | 1 kHz | 250 kHz | 5 MHz |
| STM-16/OC-48 | 5 kHz | 1 MHz | 20 MHz |

**Fig. 44: Jitter measurement filters for SDH/SONET bit rates**

**Jitter generator**

A jitter generator is needed for measuring jitter tolerance and the jitter transfer function. The jitter modulation generator and jitter modulator (phase modulator) circuits generate a clock signal at the desired bit rate with defined jitter. This clock signal is used to run the pattern generator that produces the digital signal. Special stressing signals (pseudo-random noise, sawtooth, etc.) can be fed to the external modulator input.

**Basics of wander measurement**

Wander measurement basically operates according to the same principles as jitter measurement. An external reference clock must be used instead of the internally generated reference clock, since phase variations of close to 0 Hz are to be measured. If this is implemented using a PLL, then the cutoff frequency of the lowpass filter must be as low as possible. The lower the cutoff frequency, then the longer the settling time obtained. For example, at a cutoff frequency of 0.0001 Hz, a settling time of several hours is obtained, which is entirely unpractical.

**O.171 and 0.172: Recommendations and device properties for jitter/wander measurement**

Adopted in 1999, ITU-T Recommendation O.172 is entitled “Jitter and Wander Measuring Equipment for Digital Systems which are Based on the Synchronous Digital Hierarchy (SDH)”. This new Recommendation takes its place alongside the much older O.171 governing jitter and wander measurements on PDH systems. O.172 is primarily oriented towards SDH, but it also considers the interfaces of PDH tributaries.
The new Recommendation defines instrument properties for measuring and generating jitter and wander. Note that O.172’s requirements for measurement accuracy are in some cases considerably tougher than those of O.171. The weighting filters so critical to measurement are also clearly described (see section “Jitter weighting”). New test applications required by the new synchronous technology are also described (e. g. pointer jitter). Table 8 shows the main differences between O.171 and O.172.

**Table 8: Comparison between O.171 and O.172**

| | **O.171** | **O.172** |
|---|---|---|
| Interfaces | Electrical interfaces up to 140 Mbit/s (PDH only) | Electrical and optical interfaces up to 10 Gbit/s (PDH, SDH, SONET) |
| Jitter meter, frequency range | 10 Hz to 3.5 MHz | 10 Hz to 20 MHz (at 2.5 Gbit/s) |
| Jitter meter, weighting filters | | More precise filter definition |
| Jitter meter, amplitude range | Up to 10 UIpp | Increased meas. range, e. g. 200 UIpp for STM-4 |
| Jitter meter, intrinsic error (fixed component) | e. g. 0.085 UIpp at 140 Mbit/s | 0.025 to 0.05 UIpp |
| Jitter generator, frequency range | Up to 3.5 MHz | Up to 20 MHz (up to 2.5 Gbit/s) |
| Pointer jitter test application | None | Description of test requirements, pointer test sequences |
| Wander meter, sampling rate (TIE) | | > 30 Hz |
| Wander meter, accuracy | | ± 5 % (variable component) ± 2.5 ns (fixed component) for small observation intervals |
| MTIE/TDEV algorithm | | Description with accuracy requirements |
| Wander generator, amplitude range | < 3000 UI | < 230400 UI |
| Wander generator, frequency range | > 12 µHz at 2 Mbit/s | > 12 µHz at all rates |

# Appendix: Standards for jitter and wander

To allow problem-free interconnection of different network elements in a telecommunications network, it is necessary to satisfy maximum jitter and wander amplitude criteria at the interfaces. On the other hand, inputs must tolerate a certain amount of jitter and wander. The accumulation of jitter in a chain of regenerators must be limited by compliance with jitter transfer functions. This is the reason behind the requirements stipulated for all digital hierarchy levels in the standards of the ITU-T, ANSI and ETSI.

**Table 1: Output jitter requirements for network interfaces**

| Network interface | Standard | Bit rate | Jitter limits | |
|---|---|---|---|---|
| | | | Wide-band jitter/UIpp | High-band jitter/UIpp |
| SDH transport | ITU-T G.825<br>ETSI EN 302 084 | STM-1e | 1.5 | 0.075 |
| | | STM-1 | 1.5 | 0.15 |
| | | STM-4 | 1.5 | 0.15 |
| | | STM-16 | 1.5 | 0.15 |
| | | STM-64 | 1.5 | 0.15 |
| SONET transport | ANSI T1.105.03<br>Bellcore GR-253 | OC-1 | 1.5 | 0.15 |
| | | OC-3 | 1.5 | 0.15 |
| | | OC-12 | 1.5 | 0.15 |
| | | OC-48 | 1.5 | 0.15 |
| PDH transport | ITU-T G.823<br>ETSI EN 302 084 | 2048 kbit/s | 1.5 | 0.2 |
| | | 8448 kbit/s | 1.5 | 0.2 |
| | | 34368 kbit/s | 1.5 | 0.15 |
| | | 139264 kbit/s | 1.5 | 0.075 |
| | ANSI T1.102<br>Bellcore GR-499<br>ITU-T G.824 | 1544 kbit/s | 5 | 0.1 |
| | | 6312 kbit/s | 3 (NOTE 1) | 0.1 |
| | | 44736 kbit/s | 5 | 0.1 |
| Synchronization | ITU-T G.823<br>ETS 300 462-3 | 2048 kbit/s PRC | 0.05 | - |
| | | 2048 kbit/s SSU | 0.05 | - |
| | | 2048 kbit/s SEC | 0.5 | 0.2 |
| | | 2048 kbit/s PDH | 1.5 | 0.2 |
| | ANSI T1.101 | 1544 kbit/s | 5 | 0.1 |

NOTE 1: In Draft Revised G.824: 5 UIpp

**Table 2: Output jitter requirements for equipment**

| Equipment | Standard | Bit rate | Jitter limits | |
|---|---|---|---|---|
| | | | Wide-band jitter/UIpp | High-band jitter/UIpp |
| SDH (TM, ADM, DXC etc.) | ITU-T G.813<br>ETS 300 462-5 | STM-1 | 0.5 | 0.1 |
| | | STM-4 | 0.5 | 0.1 |
| | | STM-16 | 0.5 | 0.1 |
| | ANSI T1.105.03 | OC-1 | 0.01 $UI_{rms}$ (12 kHz) | — |
| | | OC-3 | 0.01 $UI_{rms}$ (12 kHz) | — |
| | | OC-12 | 0.01 $UI_{rms}$ (12 kHz) | — |
| | | OC-48 | 0.01 $UI_{rms}$ (12 kHz) | — |
| | Bellcore GR-253 | OC-1 | 0.1 (0.01 $UI_{rms}$) | — |
| | | OC-3 | 0.1 (0.01 $UI_{rms}$) | — |
| | | OC-12 | 0.1 (0.01 $UI_{rms}$) | — |
| | | OC-48 | 0.1 (0.01 $UI_{rms}$) | — |
| SDH regenerators | ITU-T G.783<br>NOTE 1 | STM-1 | 0.3 | 0.1 |
| | | STM-4 | 0.3 | 0.1 |
| | | STM-16 | 0.3 | 0.1 |
| PRC clock | ITU-T G.811<br>ETS 300 462-6 | 2048 kbit/s | 0.05 | — |
| | | 1544 kbit/s | 0.015 | — |
| SSU clock | ITU-T G.812<br>ETS 300 462-4 | STM-1e | 0.5 | 0.075 |
| | | STM-1 | 0.5 | 0.1 |
| | | STM-4 | 0.5 | 0.1 |
| | | STM-16 | 0.5 | 0.1 |
| | | 2048 kbit/s | 0.05 | — |
| | | 1544 kbit/s | 0.05 | — |
| PDH | ITU-T G.735 | 2048 kbit/s | 0.05 | — |
| | ITU-T G.742 | 8448 kbit/s | 0.05 | — |
| | ITU-T G.751 | 34368 kbit/s | 0.05 | — |
| | | 139264 kbit/s | 0.05 | — |

NOTE 1: Revised Draft G.783 (10/98)

| Aspect | Application | ITU-T | ANSI | Bellcore | ETSI |
|---|---|---|---|---|---|
| **Output jitter/wander network interfaces** | SDH | G.825 | — | — | EN 302 084 |
| | SONET | —— | T1.105.03 | GR-253 | — |
| | PDH 1.5 Mbit/s hierarchy | —— | T1.102 | GR-499 | — |
| | PDH 2 Mbit/s hierarchy | G.823 | — | — | EN 302 084 |
| | Synchronization | G.823 | T1.101 | — | ETS 300 462-3 |
| **Output jitter/wander equipment interfaces** | SDH / SONET (TM, ADM, DXC etc.) | G.813 | T1.105.03 | GR-253 | ETS 300 462-5 |
| | SDH / SONET regenerators | G.783 (G.958) | — | — | — |
| | PRC clock | G.811 | — | — | ETS 300 462-6 |
| | SSU clock | G.812 | — | — | ETS 300 462-4 |
| | PDH | G.735<br>G.742<br>G.751 | — | — | — |
| **Mapping / pointer (combined) jitter** | SDH / SONET equipment | G.783 | T1.105.03 | GR-253 | ETS 300 417-1-1 |
| **Jitter/wander tolerance** | SDH / SONET | G.825 | T1.105.03 | GR-253 | EN 302 084 |
| | PDH 1.5 Mbit/s hierarchy | G.824 | T1.403<br>T1.404 | GR-499 | — |
| | PDH 2 Mbit/s hierarchy | G.823 | — | — | EN 302 084 |
| **Jitter/wander transfer** | SDH / SONET | G.783 (G.958) | T1.105.03 | GR-253 | — |
| | PDH 1.5 Mbit/s hierarchy (MUXDEM) | — | | GR-499 | — |
| | PDH 2 Mbit/s hierarchy (MUXDEM) | G.735 to 739<br>G.751 | — | — | — |
| **Definitions and terminology** | Synchronization networks | G.810 | — | — | ETS 300 462-1 |
| **Jitter/wander measurement equipment** | PDH equipment | O.171 | — | — | — |
| | SDH equipment | O.172 | — | — | — |

**Table 3: Jitter/wander standards**

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Printed in Germany